CX20524

Mixed Signal Device for GSM and GPRS Applications

The CX20524 Mixed Signal Device (MSD) is a highly integrated device designed for use in multi-band Global System for Mobile communications® (GSM®) and General Packet Radio Service (GPRS) handsets. The MSD includes all the power management, voice-band, mixed signal, and radio control functions required in a GSM/GPRS handset and module.

In the receive path, the MSD digitizes the baseband In-Phase/Quadrature (I/Q) inputs. Digital samples are then sent to the Baseband Processor (BP) via the Rx serial interface. The receive path features a programmable gain amplifier (PGA) for Automatic Gain Control (AGC) of the receive signal.

In the transmit path, bursts of digital data are input to the MSD over the control port. A Gaussian Minimum-Shift Keying (GMSK) modulator generates modulated I and Q waveforms from the input data. The I and Q waveforms are converted into analog waveforms and output from the MSD.

The CX20524 generates an analog signal to control the handset Power Amplifier (PA) output level.

The device voiceband Codec section provides an interface to a 32 Ω handset speaker and microphone. Line In/Out signals are also available to interface with audio accessories, such as a headset or car kit.

The MSD is designed to operate directly from a single cell, 3.6 V Li Ion battery with no external regulation required. The MSD integrates all necessary Low Drop Out (LDO) voltage regulators that generate the required device and system power supplies from battery input.

An integrated SIM interface circuit allows direct interface to 3.0 V and 1.8 V SIM cards with no external components.

An integrated battery charger control circuit provides charging capabilities for multi-chemistry batteries.

Figure 1 shows a typical CX20524 application in a handset design. The CX20524 is packaged in a compact, 160-pin (12mm x 12mm) Fine Pitch Ball Grid Array (FPBGA), Figure 2. Table 1 lists the CX20524 pin assignments.

Features

- Supports multi-slot GPRS up to Class 12
- ΣΔ Analog-to-Digital Converters (ADCs) for digitization of baseband receive signal
- Receive path PGA for AGC of received signal
- GMSK Digital Modulator
- Digital-to-Analog Converters (DACs) for analog conversion of the GMSK modulator output
- Transmit power ramping and power level control
- Low noise voiceband ADC for direct interface to handset and headset microphone
- Low noise voiceband DAC for direct interface to handset and headset speaker
- Auxiliary 8-bit ADC for monitoring system signals
- 3 V / 1.8 V SIM card interface
- Temperature sensor
- High speed asynchronous serial ports for interface to Skyworks Baseband Processor device
- Low speed asynchronous serial port for power management functions
- Voltage regulators for both internal (fixed voltage) and system (programmable voltage) needs
- Low power operation
- Control circuit for multi-chemistry advanced battery charger
- Power-On Reset (POR) generation
- Over current-limiting
- Power On/Off control inputs
- 160-pin FPBGA 12 mm x 12 mm package

Applications

- GSM handsets and modules (850/900/1800/1900 MHz)
- GPRS handsets and modules (850/900/1800/1900 MHz)

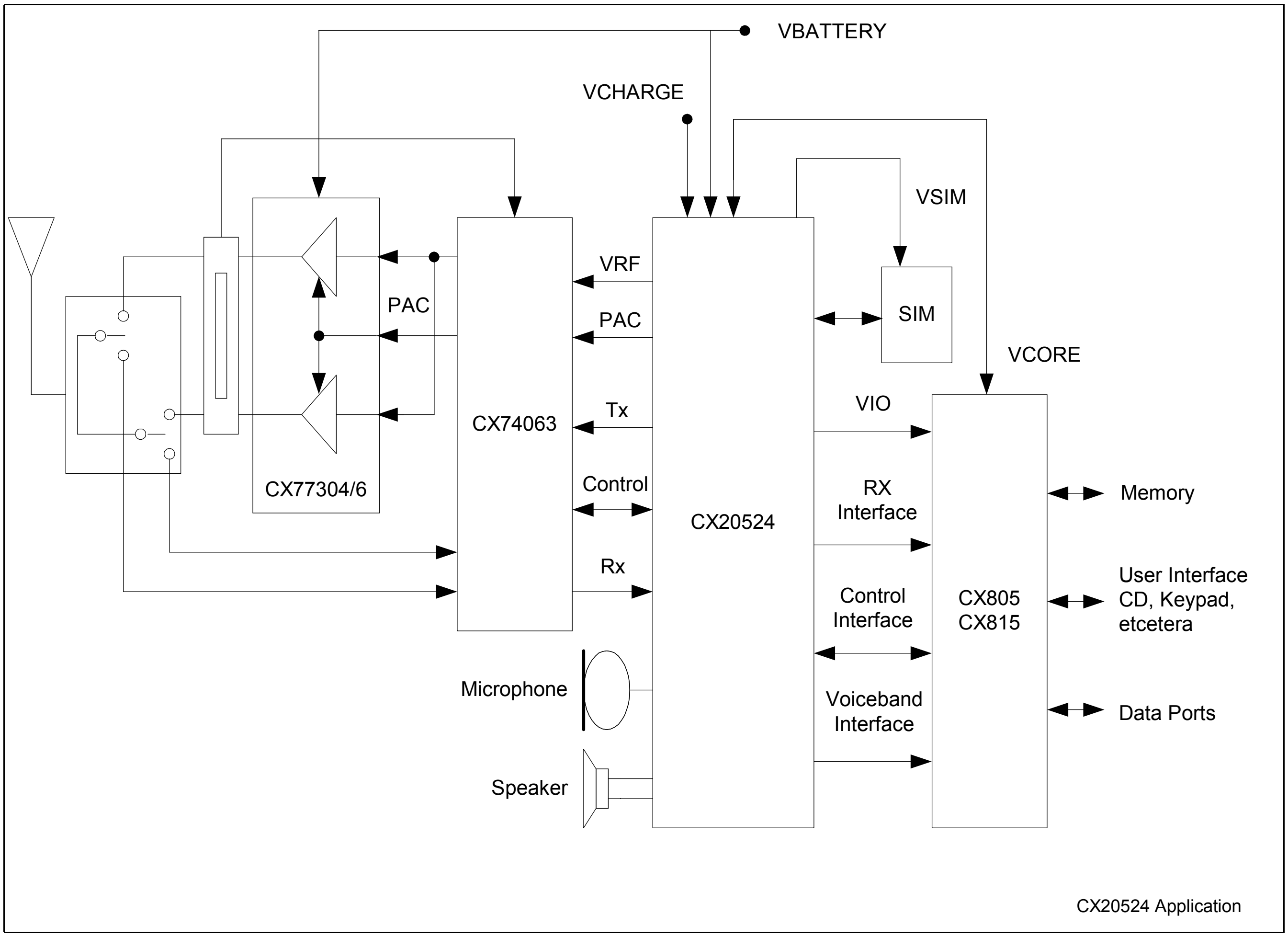
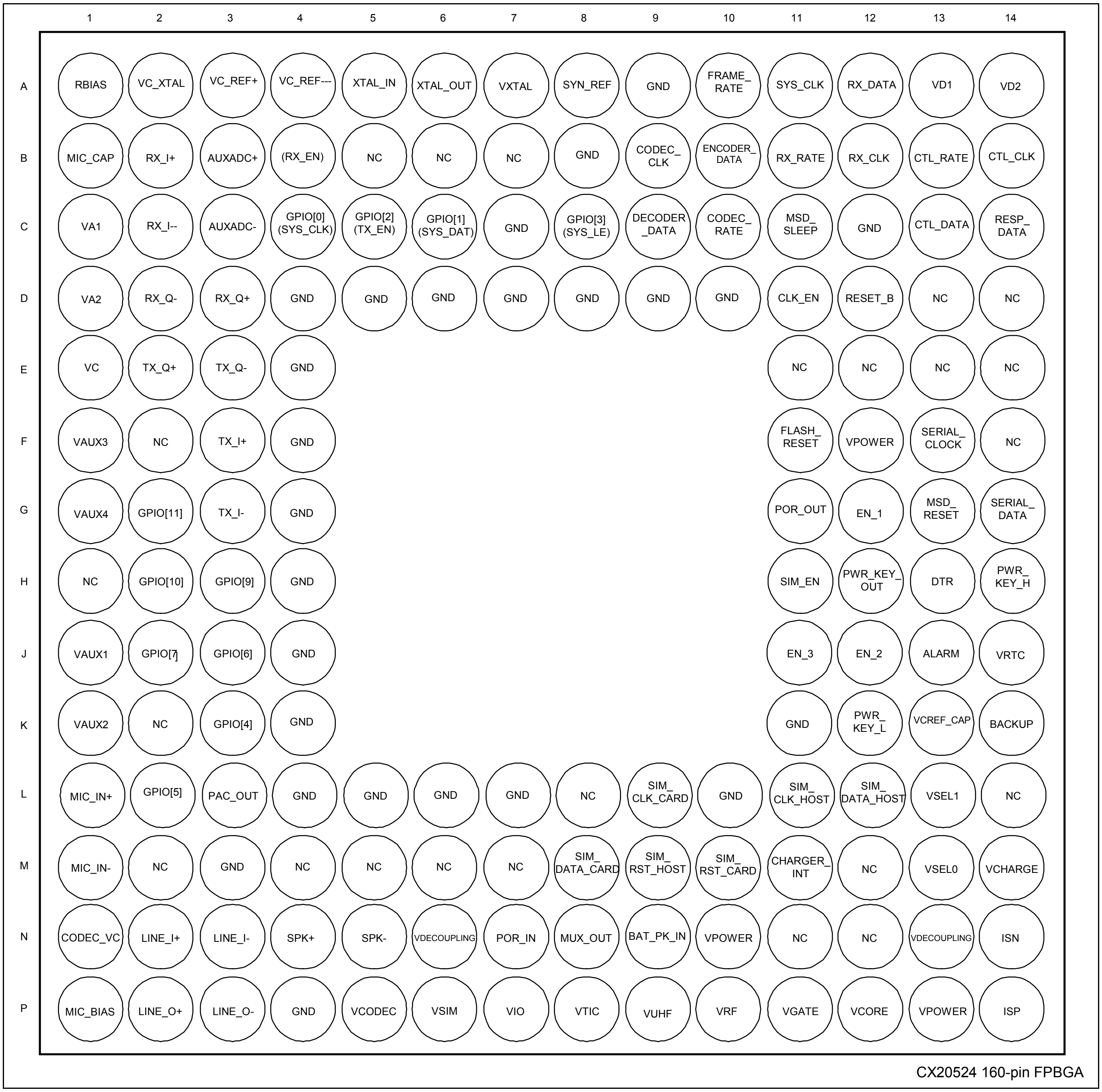


Figure 1. Typical CX20524 Application in a Handset Design



	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	RBIAS	VC_XTAL	VC_REF+	VC_REF---	XTAL_IN	XTAL_OUT	VXTAL	SYN_REF	GND	FRAME_RATE	SYS_CLK	RX_DATA	VD1	VD2
B	MIC_CAP	RX_I+	AUXADC+	(RX_EN)	NC	NC	NC	GND	CODEC_CLK	ENCODER_DATA	RX_RATE	RX_CLK	CTL_RATE	CTL_CLK
C	VA1	RX_I--	AUXADC-	GPIO[0] (SYS_CLK)	GPIO[2] (TX_EN)	GPIO[1] (SYS_DAT)	GND	GPIO[3] (SYS_LE)	DECODER_DATA	CODEC_RATE	MSD_SLEEP	GND	CTL_DATA	RESP_DATA
D	VA2	RX_Q-	RX_Q+	GND	GND	GND	GND	GND	GND	GND	CLK_EN	RESET_B	NC	NC
E	VC	TX_Q+	TX_Q-	GND							NC	NC	NC	NC
F	VAUX3	NC	TX_I+	GND							FLASH_RESET	VPOWER	SERIAL_CLOCK	NC
G	VAUX4	GPIO[11]	TX_I-	GND							POR_OUT	EN_1	MSD_RESET	SERIAL_DATA
H	NC	GPIO[10]	GPIO[9]	GND							SIM_EN	PWR_KEY_OUT	DTR	PWR_KEY_H
J	VAUX1	GPIO[7]	GPIO[6]	GND							EN_3	EN_2	ALARM	VRTC
K	VAUX2	NC	GPIO[4]	GND							GND	PWR_KEY_L	VCREF_CAP	BACKUP
L	MIC_IN+	GPIO[5]	PAC_OUT	GND	GND	GND	GND	NC	SIM_CLK_CARD	GND	SIM_CLK_HOST	SIM_DATA_HOST	VSEL1	NC
M	MIC_IN-	NC	GND	NC	NC	NC	NC	SIM_DATA_CARD	SIM_RST_HOST	SIM_RST_CARD	CHARGER_INT	NC	VSEL0	VCHARGE
N	CODEC_VC	LINE_I+	LINE_I-	SPK+	SPK-	VDECOUPLING	POR_IN	MUX_OUT	BAT_PK_IN	VPOWER	NC	NC	VDECOUPLING	ISN
P	MIC_BIAS	LINE_O+	LINE_O-	GND	VCODEC	VSIM	VIO	VTIC	VUHF	VRF	VGATE	VCORE	VPOWER	ISP

CX20524 160-pin FPBGA

Figure 2. 160-Pin FPBGA Pinout - Top View

Table 1. Pin Assignments (1 of 5)

Pin No.	Pin Name	Type	Definition	Pin No.	Pin Name	Type	Definition
A1	RBIAS	P	Resistor bias for internal references. A 30 k• 1% must be connected between this pin and ground to ensure correct device operation	H1	NC		Do not connect to this pin
A2	VC_XTAL	P	Connect 100 nF cap to ground	H2	GPO[10]	O	General Purpose Output 10
A3	VC_REF+	P	Reference voltage positive output (typically 1.85 V)	H3	GPO[9]	O	General Purpose Output 9
A4	VC_REF-	P	Reference voltage negative output (typically 0.85 V)	H4	GND	G	Ground
A5	XTAL_IN	I	Input connection for external 19.5 MHz crystal	H11	SIM_EN	O	Input is used to control VSIM voltage regulator and the voltage translator
A6	XTAL_OUT	O	Output connection for external 19.5 MHz crystal	H12	PWR_KEY_OUT	O	This signal goes low when either PWR_KEY_L or PWR_KEY_H are asserted
A7	VXTAL	P	Crystal oscillator supply output decoupling. Connect 100 nF cap to Ground	H13	DTR	I	External power on signal input (active low)
A8	SYN_REF	O	13 MHz reference output for synthesizer	H14	PWR_KEY_H	I	Power on Key input (active high)
A9	GND	G	Ground	J1	VAUX1	P	12 mA auxiliary regulator. Connect a 100 nF capacitor to ground. Reserved for future use.
A10	FRAME_RATE	O	GSM Frame Rate output	J2	GPO[7] (SYN_EN)	O	General Purpose Output 7.
A11	SYS_CLK	O	3.9 MHz System Clock output	J3	GPO[6] (PAC_OFFSET)	O	General Purpose Output 6.
A12	RX_DATA	O	Receive serial port data signal	J4	GND	G	Ground
A13	VD1	P	Digital supply output decoupling. Connect 100 nF cap to Ground. Active on power up	J11	EN_3	I	Real time input control signal #3 for controlling the LDO's (VRF, VUHF, & VTIC).
A14	VD2	P	Digital supply output decoupling. Connect 100 nF cap to Ground. Active on power up	J12	EN_2	I	Real time input control signal #2 for controlling the LDO's (VRF, VUHF, & VTIC)
B1	MIC_CAP	P	Connection pin for MIC_BIAS decoupling capacitor. Connect 100 nF cap to ground.	J13	ALARM	I	Internal pull-up is connected to VRTC. Alarm power on signal input (active low).
B2	RX_I+	I	I Channel Baseband Rx signal (positive)	J14	VRTC	P	Isolated voltage regulator, this regulator is always ON, even when the MSD is OFF
B3	AUXADC+	I	Auxiliary ADC positive input	K1	VAUX2	P	5 mA auxiliary regulator. Connect a 100 nF capacitor to Ground. Reserved for future use.
B4	GPO[8] (RX_EN)	O	General Purpose Output 8.	K2	NC		Do not connect
B5	NC		Do not connect to this pin	K3	GPO[4] (VC1)	O	General Purpose Output 4.
B6	NC		Do not connect to this pin	K4	GND	G	Ground

Table 1. Pin Assignments (2 of 5)

Pin No.	Pin Name	Type	Definition	Pin No.	Pin Name	Type	Definition
B7	NC		Do not connect to this pin	K11	GND	G	Ground
B8	GND	G	Ground	K12	PWR_KEY_L	I	Power on key input (active low).
B9	CODEC_CLK	I	Codec serial port clock signal	K13	VCREF_CAP	P	Internal bandgap (output connect 10 nF to ground.
B10	ENCODER_DATA	I	Codec serial port encoder data signal	K14	BACKUP	P	Back-up Battery input
B11	RX_RATE	O	Receive serial port word rate signal	L1	MIC_IN+	I	Microphone positive input
B12	RX_CLK	O	Receive serial port clock	L2	GPO[5] (VC2)	O	General Purpose Output 5
B13	CTL_RATE	I	Control serial port word rate signal	L3	PAC_OUT	O	Power Control Loop output
B14	CTL_CLK	O	Control serial port clock	L4	GND	G	Ground
C1	VA1	P	Baseband analog supply output decoupler. Connect to pin D1. Connect a 100 nF capacitor to ground.	L5	GND	G	Ground
C2	RX_I-	I	I Channel Baseband Rx signal (negative)	L6	GND	G	Ground
C3	AUXADC-	I	Auxiliary ADC negative input	L7	GND	G	Ground
C4	GPO[0] (SYS_CLK)	O	General Purpose Output 0.	L8	NC		Do not connect to this pin
C5	GPO[2] (TX_EN)	O	General Purpose Output 2.	L9	SIM_CLK_ CARD	O	Un-buffered SIM clock signal connected to the SIM card
C6	GPO[1] (SYS_DAT)	O	General Purpose Output 1.	L10	GND	G	Ground
C7	GND	G	Ground	L11	SIM_CLK_ HOST	I	Buffered SIM clock signal connected to HOST
C8	GPO[3] (SYS_LE)	O	General Purpose Output 3.	L12	SIM_DATA_ HOST	I/O	Buffered SIM data signal connected to the HOST
C9	DECODER_DATA	I	Codec serial port decoder data	L13	VSEL1	I	VRTC and VCORE voltage selection pin
C10	CODEC_RATE	O	Codec serial port word rate	L14	NC		Do not connect to this pin
C11	MSD_SLEEP	I	Forces the MSD to enter sleep state (low current) and is connected to pin D11 CLK_EN	M1	MIC_IN-	I	Microphone negative input
C12	GND		Reserved. Connect to ground	M2	NC		Do not connect to this pin
C13	CTL_DATA	I/O	Control serial port serial data signal (bi-directional)	M3	GND	G	Ground
C14	RESP_DATA	O	Control serial port response data signal	M4	NC		Do not connect to this pin

Table 1. Pin Assignments (3 of 5)

Pin No.	Pin Name	Type	Definition	Pin No.	Pin Name	Type	Definition
D1	VA2	P	Receive/transmit output decoupler. Connect to pin C1. Connect a 100 nF capacitor to ground	M5	NC		Do not connect to this pin
D2	RX_Q-	I	Q Channel Baseband Rx signal (negative)	M6	NC		Do not connect to this pin
D3	RX_Q+	I	Q Channel Baseband Rx signal (positive)	M7	NC		Do not connect to this pin
D4	GND	G	Ground	M8	SIM_DATA_ CARD	I/O	Un-buffered SIM data signal connected to the SIM card
D5	GND	G	Ground	M9	SIM_RST_HOST	I	Buffered SIM reset signal connected to the HOST
D6	GND	G	Ground	M10	SIM_RST_CAR D	O	Un-buffered SIM reset signal connected to the SIM card
D7	GND	G	Ground	M11	CHARGER_INT	O	A high on this pin will indicate to the Host the presence of a charger
D8	GND	G	Ground	M12	NC		Do not connect to this pin
D9	GND	G	Ground	M13	VSEL0	O	VRTC and VCORE voltage selection pin
D10	GND	G	Ground	M14	VCHARGE	P	External charging voltage input
D11	CLK_EN	I	Clock request input. Connect to pin C11	N1	VC_CODEC	P	Codec bias reference voltage. Connect a 100 nF capacitor to ground.
D12	RESET_B	O	Baseband reset signal	N2	LINE_I+	O	Line In positive input
D13	NC		Do not connect to this pin	N3	LINE_I-	O	Line In negative input
D14	NC		Do not connect to this pin	N4	SPK+	O	Speaker positive output
E1	VC		Bias reference voltage. Connect a 100 nF capacitor to ground.	N5	SPK-	O	Speaker negative output
E2	TX_Q+	O	Q Channel Baseband Tx signal (positive)	N6	VDECOUPLING	P	Connect to pin N13
E3	TX_Q-	O	Q Channel Baseband Tx signal (negative)	N7	POR_IN	O	Power on reset signal. Connect to G11
E4	GND	G	Ground	N8	MUX_OUT	O	Analog MUX output, connect to AUX_ADC
E11	NC		Do not connect to this pin	N9	BAT_PK_IN	I	Analog input used to detect the battery pack size (there is an internal voltage divider on chip)
E12	NC		Do not connect to this pin	N10	VPOWER	P	MSD input voltage pin. Connect to pin P13
E13	NC		Do not connect to this pin	N11	NC		Do not connect to this pin

Table 1. Pin Assignments (4 of 5)

Pin No.	Pin Name	Type	Definition	Pin No.	Pin Name	Type	Definition
E14	NC		Do not connect to this pin	N12	NC		Do not connect to this pin
F1	VAUX3	P	5 mA auxiliary regulator. Connect a 100 nF capacitor to ground. Reserved for future use	N13	VDECOUPLING	P	Connect to pin N6 and to 33 μF capacitor to ground
F2	NC		Do not connect to this pin	N14	ISN	I	Battery Side of the internal current sense resistor (0.10 • typical)
F3	TX_I+	O	I Channel Baseband Tx signal (positive)	P1	MIC_BIAS	P	Microphone bias voltage (output)
F4	GND		Ground	P2	LINE_O+	O	Audio Line Out positive input
F11	FLASH_RESET	O	Flash Memory Reset signal. Active while POR and CLK_REQ	P3	LINE_O-	O	Audio Line Out negative output
F12	VPOWER	P	MSD input voltage pin. Connect to pin N10 and P13	P4	GND	G	Ground
F13	SERIAL_CLOCK	O	Low speed asynchronous serial port clock	P5	VCODEC	P	Codec section analog output decoupling. Connect a 100 nF capacitor to ground
F14	NC		Do not connect to this pin	P6	VSIM	P	SIM card voltage supply
G1	VAUX4	P	5 mA auxiliary regulator. Connect a 100 nF capacitor to ground. Reserved for future use.	P7	VIO	P	Dedicated digital circuit supply for the I/O pads and associated external circuits, this regulator is ON by default whenever the MSD is turned ON
G2	GPO[11]	O	General Purpose Output 11	P8	VTIC	P	100 mA regulator dedicated to the translation loop, controlled by either the real time control pins or by the override register
G3	TX_I-	O	I Channel Baseband Tx signal (negative)	P9	VUHF	P	50 mA regulator dedicated to the UHF VCO and buffers, controlled by either the real time control pins or by the override register
G4	GND	G	Ground	P10	VRF	P	150 mA regulator for main RF supply, controlled by either the real time control pins or by the override register

Table 1. Pin Assignments (5 of 5)

Pin No.	Pin Name	Type	Definition	Pin No.	Pin Name	Type	Definition
G11	POR_OUT	O	This is the system power on reset output signal. Connect to pin N7	P11	VGATE	O	Output signal controlling the gate of the external pass FET used for the battery charger
G12	EN_1	I	Real time input control signal #1 for the LDOs (VRF, VUHF, & VTIC)	P12	VCORE	O	Dedicated baseband Core digital supply, this regulator is ON by default whenever the MSD is turned ON
G13	MSD_RESET	I	Falling edge resets MSD and turns it off	P13	VPOWER	P	MSD input voltage pin. Connect to pin N10 and F12
G14	SERIAL_DATA	I/O	Low speed serial port bi-directional data	P14	ISP	I	Charger side of the internal current sense resistor (0.10 • typical)
Types: P = Power G = Ground O = Output I = Input I/O = Input/Output							

Technical Description

Overview

The CX20524 (Figure 3) consists of the following functional areas:

- Receiver
- Transmitter
- TX Power Control
- Timing Generation and Control
- Synthesizer Interface
- Voiceband Codec
- Auxiliary ADC
- Temperature Sensor
- General Purpose Outputs
- Power Management
- Battery Charger and Monitor
- SIM Card Interface
- Low Speed Asynchronous Serial Port
- Watch Dog
- Sleep Mode

Receiver

The MSD receiver converts the received baseband analog signal into digital samples for processing by the BP. The MSD receiver path consists of the following blocks:

- Programmable Gain Amplifier
- Sigma-Delta (ΣΔ) ADC
- Receive Interface

Programmable Gain Amplifier

The Programmable Gain Amplifier (PGA) amplifies the input baseband signal. The PGA gain is programmable in 6 dB steps from 0 dB to 12 dB and is controlled by register 0C0h.

ΣΔ ADC

The ΣΔ ADC samples the amplified PGA baseband signal at a rate of 9.75 Msps. The ADC-produced digital samples are a quadrature baseband representation of the input signal. The ADC uses ΣΔ technology to generate high-resolution 13-bit samples. The 13-bit samples are left justified in 16-bit words. The In-Phase/Quadrature (I/Q) samples produced are output from the ADC at a rate of 1.083 Msps. This corresponds to an I/Q pair sample rate of 540 ksps, which is twice the GSM bit rate of 270 kbps.

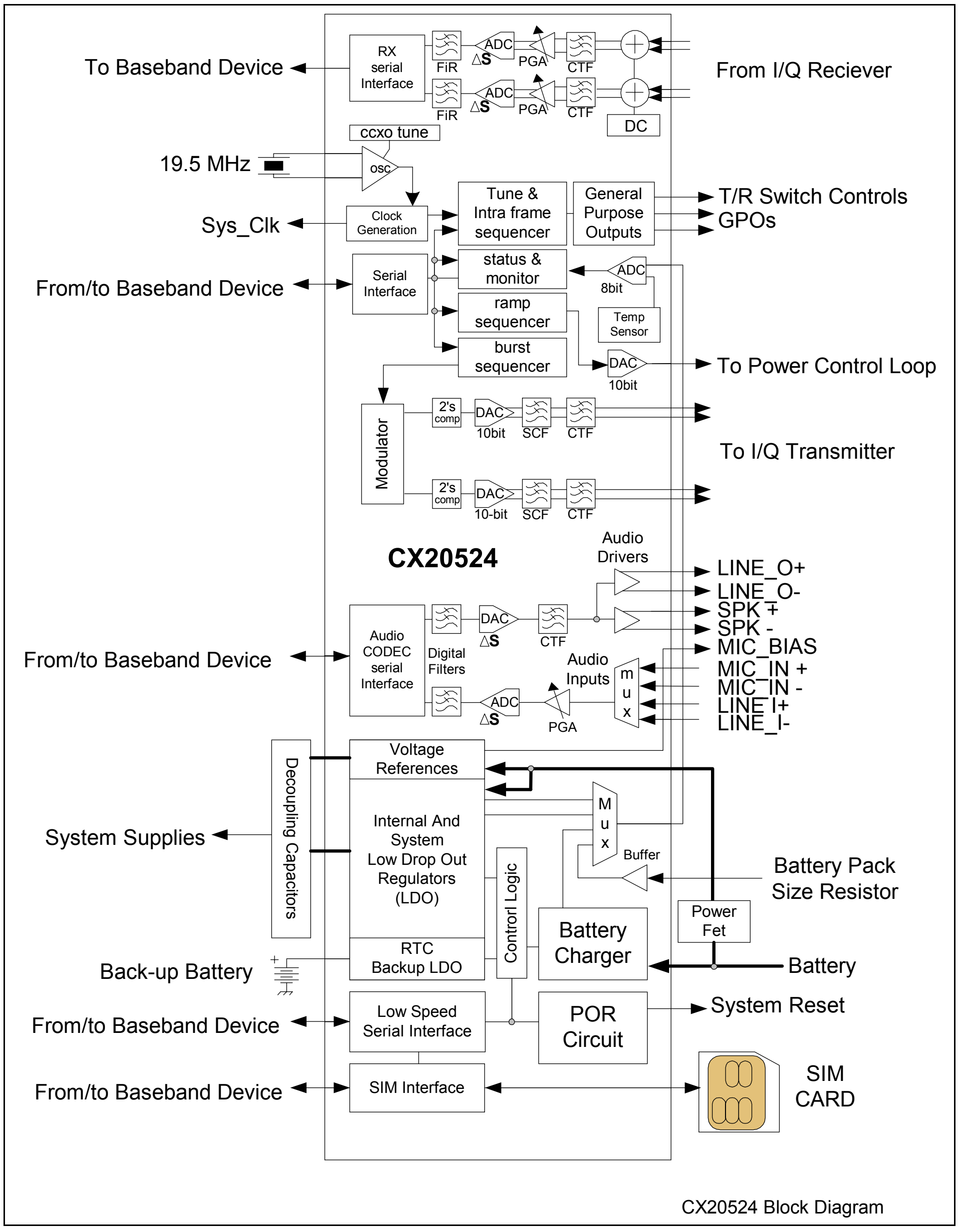


Figure 3. CX20524 Block Diagram

Receive Interface

ADC-generated I/Q samples are sent out from the MSD on the Receive Interface. The Receive Interface is a three-wire serial interface designed to interface between the MSD and BP. The interface is a high speed, synchronous, simplex, serial communications link. The interface signals include the following:

- RX_CLK. 19.5 MHz output clock
- RX_RATE. 1.083 MHz output clock that indicates the start of a word on the RX_DATA output. The RX_RATE clock pulse width is one bit period
- RX_DATA. Serial output data at 19.5 Mbps

Figure 4 shows the Receive Interface timing diagram.

The Receive Interface serial output data changes state on the clock signal rising edge. Each I or Q sample is 16-bits wide with two stuff bits between samples. The RX_RATE signal indicates when a new I or Q sample is starting.

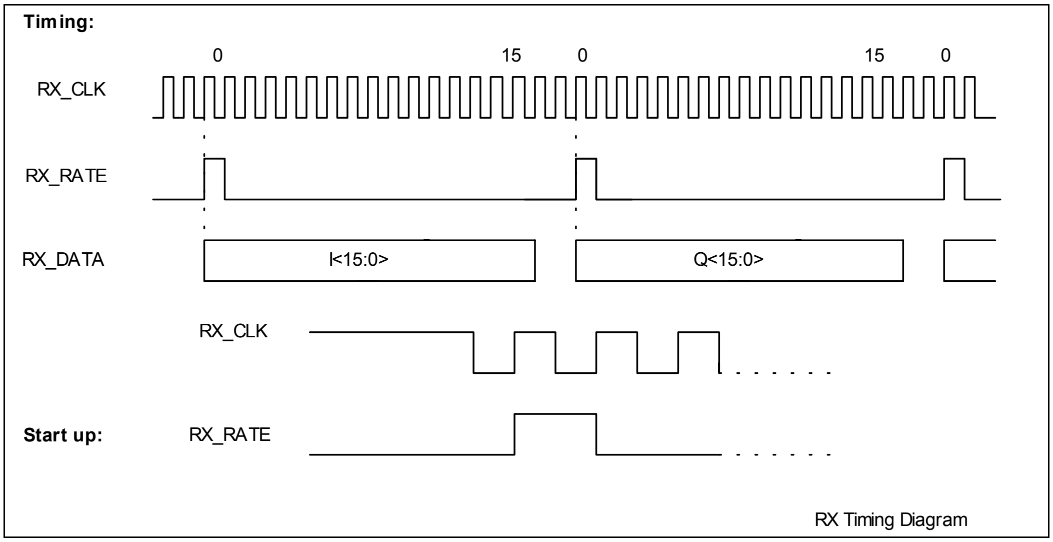


Figure 4. Receive Interface Timing Diagram

Transmitter

The MSD transmitter:

- Buffers the baseband transmit data
- Performs GMSK data modulation
- Generates analog I/Q output signals for the RF subsystem

The MSD Transmit path contains the following blocks:

- Burst Store RAM
- Gaussian Minimum-Shift Keying (GMSK) Modulator
- I/Q DACs
- I/Q Reconstruction Filters
- I/Q DC Offset and Gain/Phase Imbalance Adjust

Burst Store RAM

The Burst Store RAM is used to store transmit data. It consists of a bank of 32×16-bit registers. These registers are written to using the MSD Control Interface. The Burst Store RAM address is 0E0 to 0FFh. When the Intra-Frame Sequencer (IFS) bit 14 = 1, the Burst Store RAM contents are shifted out serially to the GMSK modulator. As long as bit 14 remains set to 1, data continues to be shifted out to the GMSK modulator. The data is shifted out starting with the word in the Burst Store RAM lowest address, with the most significant bit (MSB) first. The serial output rate is 270.83 kbps. The burst store RAM is compatible with GPRS multi-slot transmission requirements.

GMSK Modulator

The GMSK modulator performs the modulation of the Burst Store RAM serial data stream. During the TDMA transmit slot, the I and Q data are generated at a rate of 4.33 Msps, which is 16-times the input data rate. Each sample is a 10-bit word. The I and Q samples are the complex representation of the GMSK waveform.

I/Q DACs

I/Q DACs convert the GMSK modulator I and Q samples from digital samples to analog signals. The conversion rate is 4.33 Msps, the same as the GMSK Modulator output data rate.

I/Q Reconstruction Filters

I/Q reconstruction filters provide low pass filtering of the analog I and Q signals from the I/Q DACs. The output of the reconstruction filters are continuous time I and Q signals. The differential I and Q outputs are available at the following MSD pins:

- TX_I+/TX_I-
- TX_Q+/TX_Q-

I/Q DC Offset and Gain/Phase Imbalance Adjust

The MSD provides adjustments to minimize the DC offset and gain/phase imbalance between I and Q transmit channels. This adjustment may be used to compensate for offsets and imbalances introduced in the RF subsystem.

I/Q DC Offset Adjust. The Tx Offset Register is used to store the I/Q DC offset adjustment value. For both I and Q channels, the contents of this 16-bit register are added to the 10-bit samples from the modulator to generate the DC-compensated samples. If no DC compensation is required, the registers are loaded with 0s. Bits 15-8 contain the I channel DC offset adjustment value, and bits 7-0 contain the Q channel DC offset adjustment value. The Tx Offset Register is located at address 0x100h.

Gain/Phase Imbalance Adjust. Gain/phase mismatch between the RF Subsystem I and Q transmit channels are compensated for in the MSD using the Tx I/Q Control Register. Bits 5-1 contain the I/Q channel relative gain adjustment value. Bits 14-10 contain the I/O phase adjustments. The Tx I/Q Control Register is located at address 0x101h.

Tx Power Control

The MSD generates a signal to control the output power level of the handset Power Amplifier (PA). The Tx Power Control circuitry in the MSD consists of the following blocks:

- Ramp Store
- Power Control DAC

Ramp Store Memory. The Ramp Store Memory is a bank of RAM consisting of 64×16-bit words. Ramp store addresses are from 80 to BFh. The Control Port is used to write to the Ramp Store Memory. At the start of a transmit slot, the PA output power must be ramped up to the required transmit power level. At the end of the transmit slot, the PA output power must be ramped back down. The ramping profile is stored in the Ramp Store Memory.

Bit 2 and bit 11 of the IFS register enable the output from the Ramp Store Memory. When bit 2 and bit 11 are set to 1 for the first time, words 0-m in the Ramp Store Memory are sequentially sent out to generate the rising edge of the ramp profile. When bit 2 and bit 11 are set to 1 for the second time, words (m + 1) through n in the Ramp Store Memory are sequentially sent out to generate the falling edge of the ramp profile. The number of words (values of m and n) used to create the rising and falling edges depend on the duration of each state in the IFS.

Bits 15-6 of each word specify the power level for that state. Bits 4-0 specify the duration of the state, as a number of 2.167 MHz clock cycles. 2.167 MHz is eight times the system bit rate (270.833 kbps). Bit 5 is reserved.

Power Control DAC. The Ramp Store outputs 10-bit data samples to the Power Control DAC. The Power Control DAC is a 10-bit DAC that converts the samples it receives from the Ramp Store into an analog signal that is output from the MSD. The signal is used to control the PA output power.

Timing Generation and Control

The Timing Generation and Control circuit consists of:

- 19.5 MHz crystal interface and clock generation
- Control Interface
- Intra-Frame Sequencer
- Synthesizer Sequencer

Timing Generation

The MSD provides an oscillator circuit that generates a reference signal from an external 19.5 MHz crystal. This reference is used to generate the following timing signals:

- Synthesizer reference clock for the RF subsystem
- System clock output for the baseband digital device
- All MSD internal circuitry timing signals

To minimize power dissipation, the oscillator circuit and the clock generation circuits can be turned off when the handset enters low power mode.

The clock generation circuit consists of the following blocks:

- Crystal oscillator circuit
- Synthesizer reference signal circuit
- System clock circuit

Crystal Oscillator Circuit. The crystal oscillator circuit features an internal oscillator function, which is used with an external crystal. The contents of two internal registers, the Oscillator Control Register (102, 103h), are used to tune the crystal oscillator frequency. The external components required are a 19.5 MHz crystal, and a bias resistor. The external output of the oscillator circuit is a 13 MHz reference signal. A circuit diagram for the internal and external components of the crystal oscillator circuit is shown in Figure 5.

Clock Startup

Clock startup timing is shown in Figure 6. On power up, the clock starts operating within 8 msec after VIO has reached 92 percent of its target value. Signals POR_IN and FLASH_RESET are released within 10-16 ms after power up. Once POR_IN is released, RESET_B signal is released in 60 µs.

CCXO

There are two digitally controlled capacitor banks at the input and output of XTAL oscillator that are controlled by the Capacitor Controlled Crystal Oscillator (CCXO). DAC Input bank is CLD1 and the output bank is CLD2 (see Figure 7). They are controlled by writing to the CCXO output control register.
Bits 15-9 are used for coarse adjustment. CCXO input control register bits 15-9 are used for coarse adjustment, bits 8-0 are for fine adjustment. CCXO DAC is a combination of switches and capacitors that are turned ON/OFF depending on the digital input word. The switched capacitor network is connected at the output and input of the XTAL oscillator to change the frequency by switching capacitors.

Digital Clock Generator

Figure 8 shows the block diagram of the digital clock generator. The digital clock generator creates and buffers all clocks for the sub-blocks. In normal operation, the clock generator gets its main clock from the XTAL oscillator block. Clocks are generated for the following digital blocks:

- Receive block. The whole receive portion runs at 19.5 MHz. Therefore the XTAL clock gets directly fed through the clock generator. Additional buffering is provided.
- Transmit block. The transmit portion runs at 4.333 MHz. The clock-generator divides the XTAL clock by 4.5 and provides it to the transmit chain.
- Power Amplifier block. The analog section of the PA runs at half the XTAL frequency. The clock generator has a divide by 2- block, which provides the clock to the analog. The digital section of the PA runs at 4.875 MHz (another divide by 2-stage is added after the analog-divider section).
- Codec block. The XTAL clock of 19.5 MHz is directly provided to the CODEC, where it is internally divided down.
- Register + Stores. All the registers and stores get loaded based on a 2.166 MHz-clock. This clock is derived from the transmit clock, which runs at half of its frequency.
- ADC Calibration. The ADC runs at 541.666 kHz, that is also derived from the transmit clock (divided by 8).

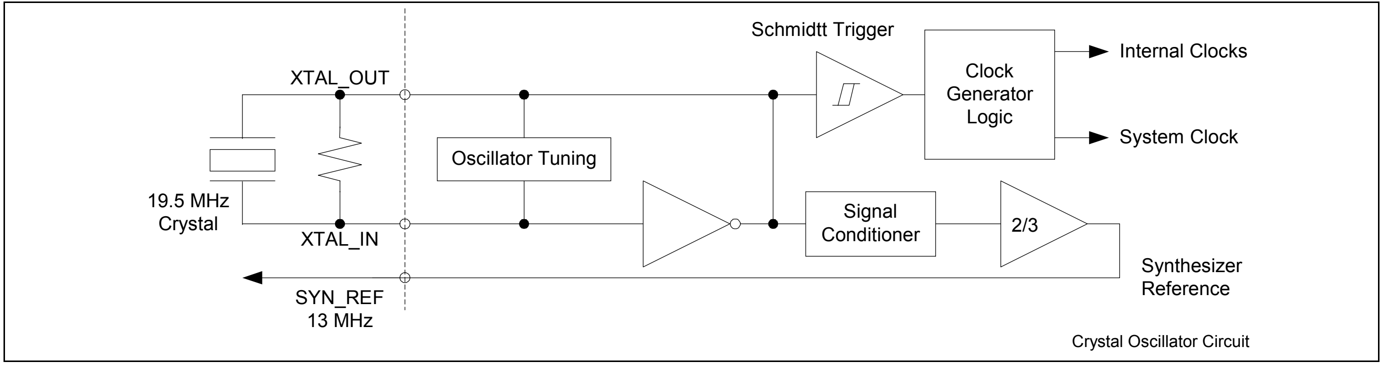


Figure 5. Crystal Oscillator Circuit Diagram

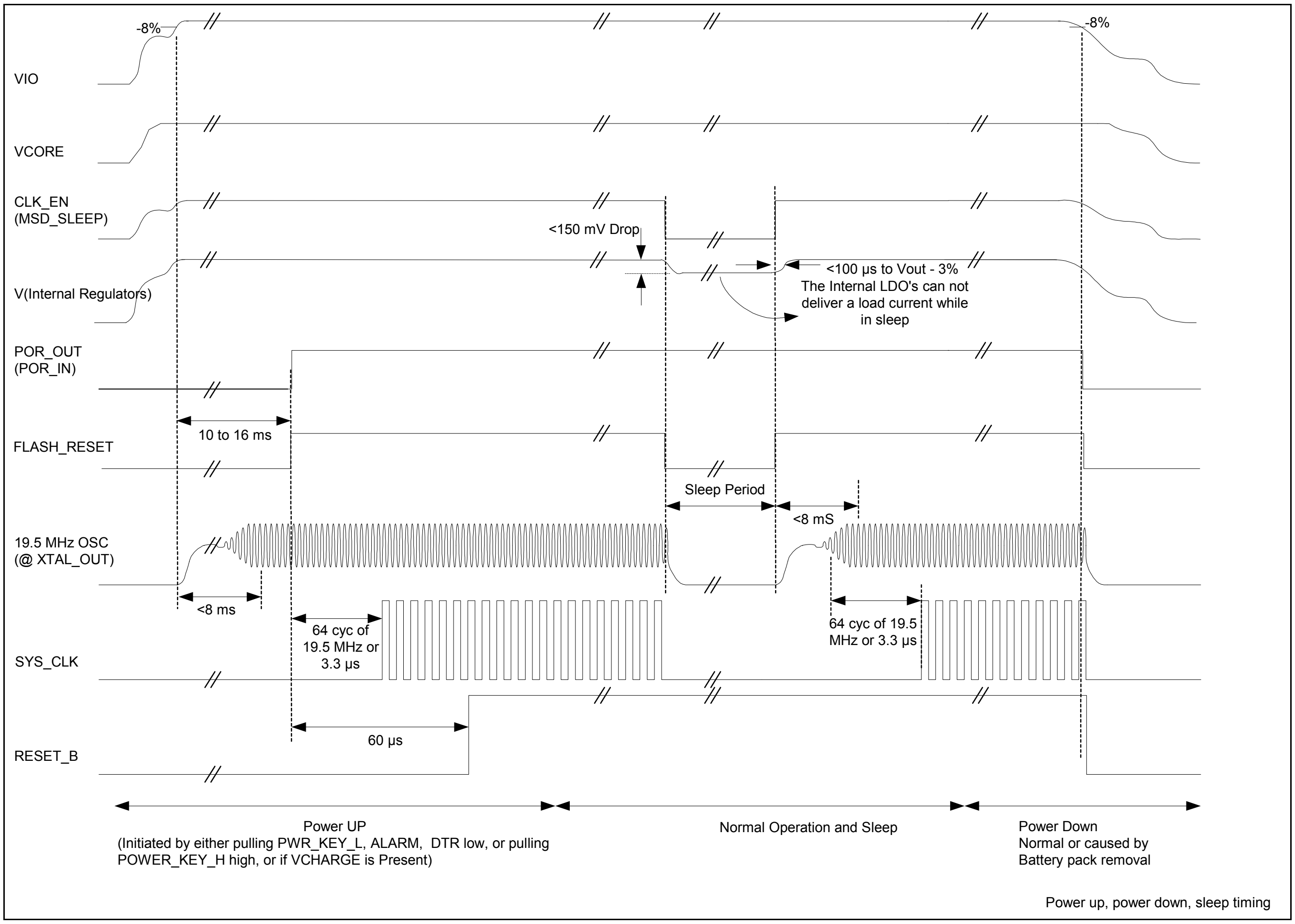


Figure 6. Clock Startup, Power Up, Power Down and Sleep Timing

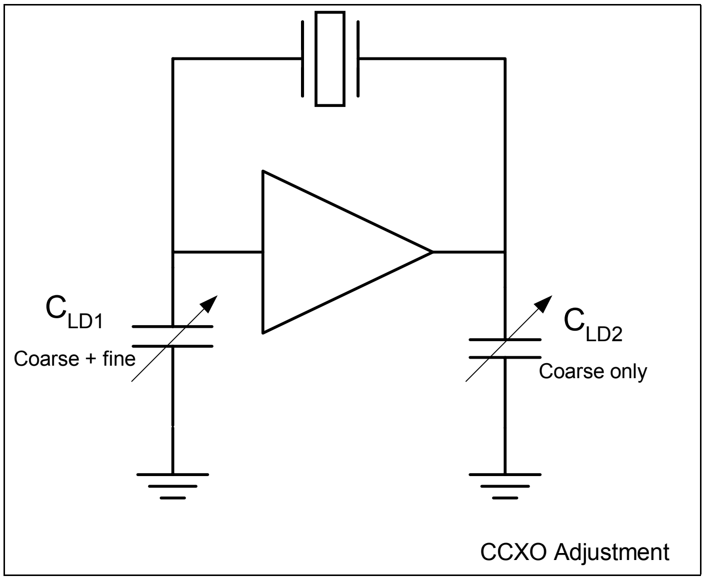


Figure 7. CCXO Adjustment

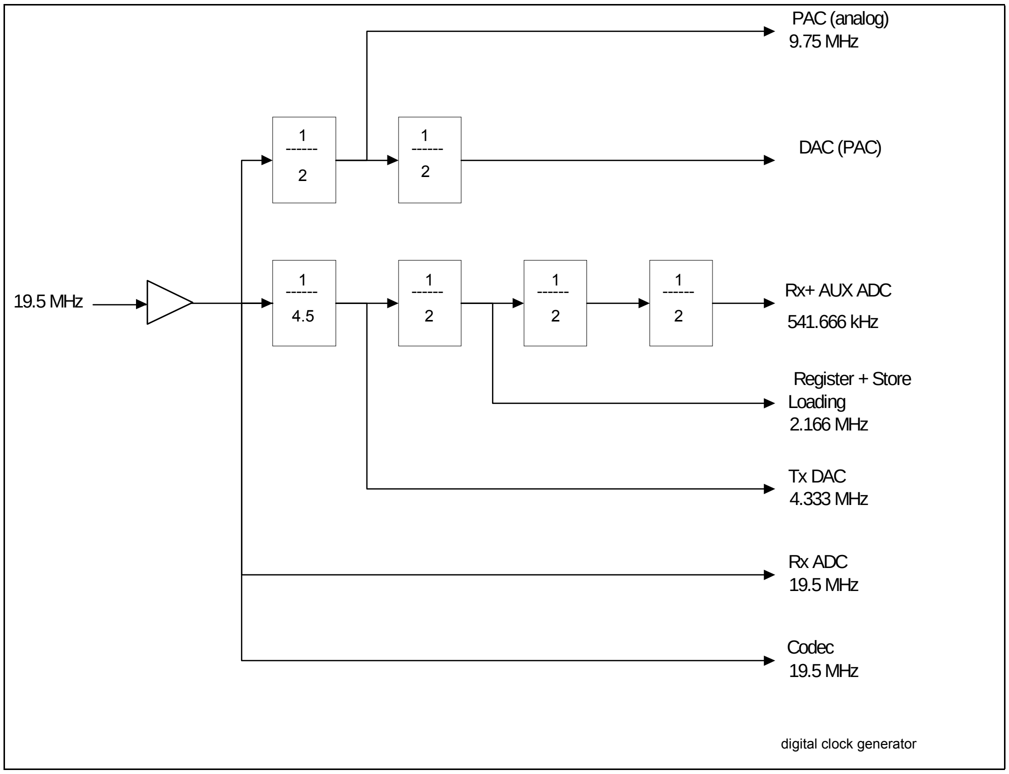


Figure 8. Digital Clock Generator

Synthesizer Reference Signal Circuit. The MSD produces a reference signal for use by the synthesizer device in the RF subsystem. A 13 MHz reference output is provided on SYN_REF (pin A8). Figure 9 shows the load circuit to be used with SYN_REF. The components may need to be adjusted for different PCB layouts.

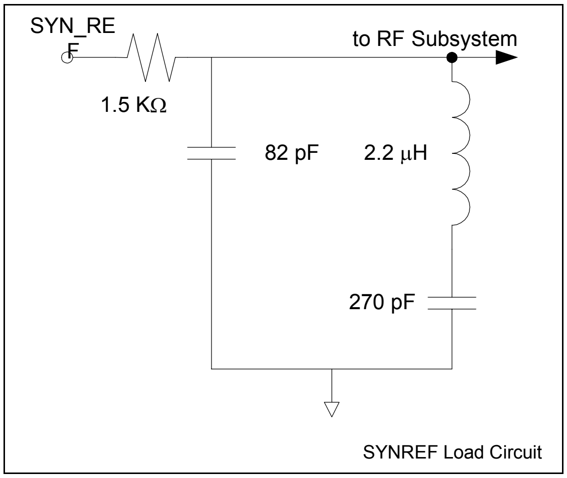


Figure 9. SYNREF Load Circuit

System Clock Circuit. The MSD generates a 3.9 MHz system clock output from the reference signal (SYS_CLK). The BP uses this system clock output for its internal timing references, when it receives a clock enable signal (CLK_EN) from the BP. The SYS_CLK uses pin A11.

Control Interface

The control interface is a four-wire serial interface, which allows the BP to control and configure the MSD. The interface is a high speed, synchronous, full duplex, serial communications link.

The control interface consists of the following signals:

- CTL_CLK. 3.9 MHz clock signal input to the MSD
- CTL_RATE. Control input signal used to indicate the start and end of a data transfer session between the BP and MSD
- CTL_DATA. Serial input data to the MSD
- RESP_DATA. Serial output data from the MSD

The BP is the bus master for the control interface and initiates all communication over the interface. The BP uses the control interface to perform the following functions:

- Send control information to configure MSD operation
- Send bursts of transmit data for modulation by the MSD
- Read contents of the MSD registers

Figure 10 shows the control interface timing diagram for write and read operations.

Intra-Frame Sequencer

The Intra-Frame Sequencer (IFS) is a programmable state machine that generates timing and control signals for the RF subsystem and internal MSD circuits. The IFS consists of a
128-word RAM (each word is 16 bits wide) that is written to the control interface. The IFS RAM is located at MSD register addresses 0x00 to 0X7Fh.

There are 64 states in the IFS, with each state controlled by two words:

- Duration Word: defines the duration of the state.
- Assertions Word: defines the logic level of each of the control signals in the state.

The duration word for each state specifies the length of the state, as a number of 2.166 MHz clock cycles (1 cycle = 0.4625 µs). This frequency is eight times the system bit rate (270.833 kbps). Bits 14-0 of the duration word specify the number of clock cycles in the state. The length of the state is calculated as follows:

$$(\text{Duration Word }[14{:}0] + 1) \times 0.4625\ \mu s$$

Bit 15 is a reset bit. If this bit is set to 1, the state machine resets to its starting state on the next 2.166 MHz clock cycle after the specified duration of the current state has expired.

The assertions word for each state specifies the logic level of each of the control signals. There are a total of 16 control signals, some of which are output from the MSD, while others are only used internally.

Synthesizer Sequencer

The synthesizer sequencer (tune store) is a programmable state machine that can be configured using the control interface. Each sequencer state consists of two 16-bit words. The data can be used to program the RF subsystem frequency synthesizer device, or to configure RF transceiver device operation. The sequencer RAM is comprised of 32×16-bit words. The sequencer RAM is located at MSD register addresses 0C0 to 0DFh.

Synthesizer sequencer operation is controlled by IFS signals. When IFS bit 2 is set to 0, the synthesizer sequencer is reset to its starting state. The sequencer remains in this state as long as bit 2 is set to 0.

If bit 2 is set to 1, that is, reset released, and bit 3 is set to 1, the synthesizer sequencer starts to send the first state of the sequencer over the synthesizer interface. Of the 32 bits stored in the first state, 24 bits are sent over the interface, and then the sequencer counts eight serial interface bit periods.

When the count expires, IFS bit 3 state is checked. If it is still set to 1, an additional 24 bits from the next synthesizer sequencer state are sent through the synthesizer interface. If bit 3 is set to 0, the sequencer waits until bit 3 is set to 1 again before proceeding to the next sequencer state.

For each synthesizer state, a 24-bit data sequence, that is, bits 31-8, is sent out on the synthesizer interface. This data may be a command for an RF frequency synthesizer device to set up the required frequency for a transmit, receive, or monitor slot. The data can also configure the various parameters of the RF subsystem devices.

Synthesizer Interface

The synthesizer interface is a three-wire serial interface for communication between the MSD and RF subsystem. The interface is a high speed, synchronous, simplex serial communications link. The synthesizer sequencer provides the data that is sent out on the synthesizer interface. The three synthesizer interface signals are:

- SYS_CLK. 3.9 MHz output clock signal.
- SYN_EN. 135.4 kHz output framing signal. This signal remains low for 24 SYS_CLK periods if the MSB of the data word is set to 0.
- SYN_DATA. Serial output data. The bit rate is 4.3 MHz. Each data word sent over the interface is 24 bits long. Eight padding bits are appended to the data word to give a frame rate of 135.4 kHz.

Figure 11 shows the synthesizer interface timing diagram.

Voiceband Codec

The Voiceband Codec includes the following sections:

- Encoder
- Decoder
- Codec Interface

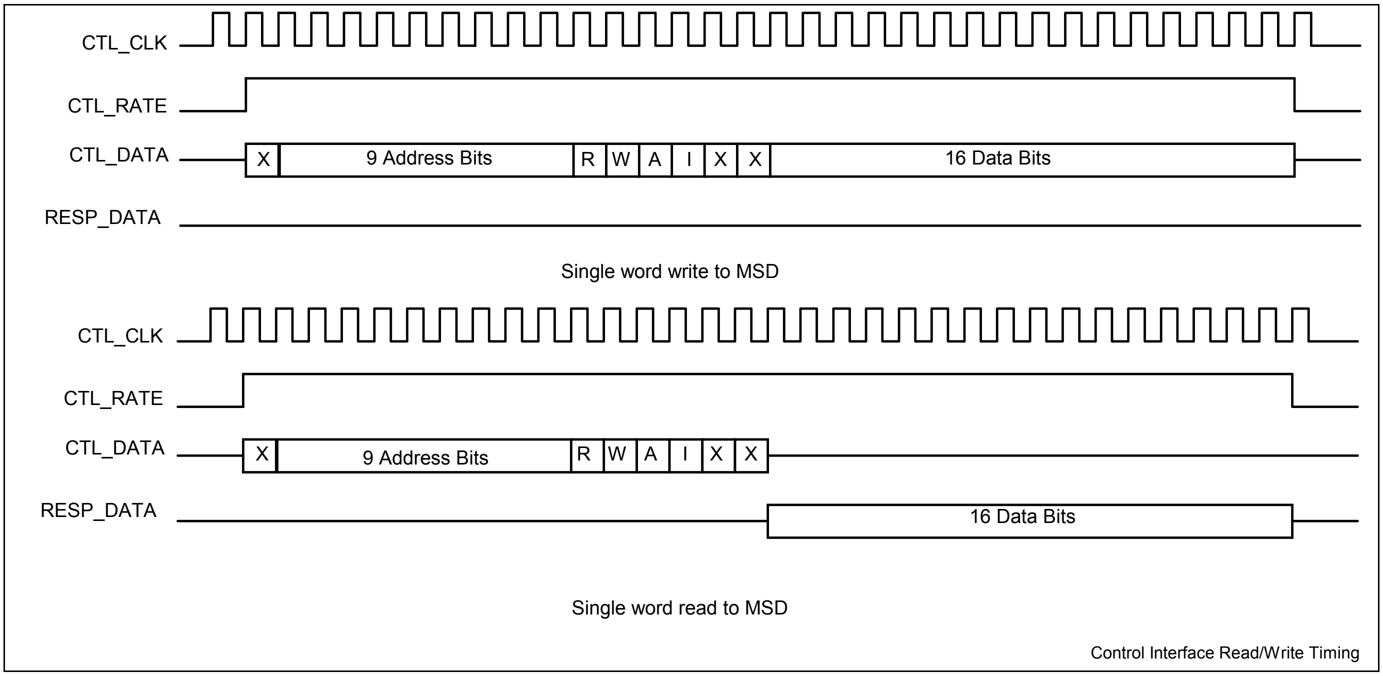


Figure 10. Control Interface Read/Write Timing Diagram

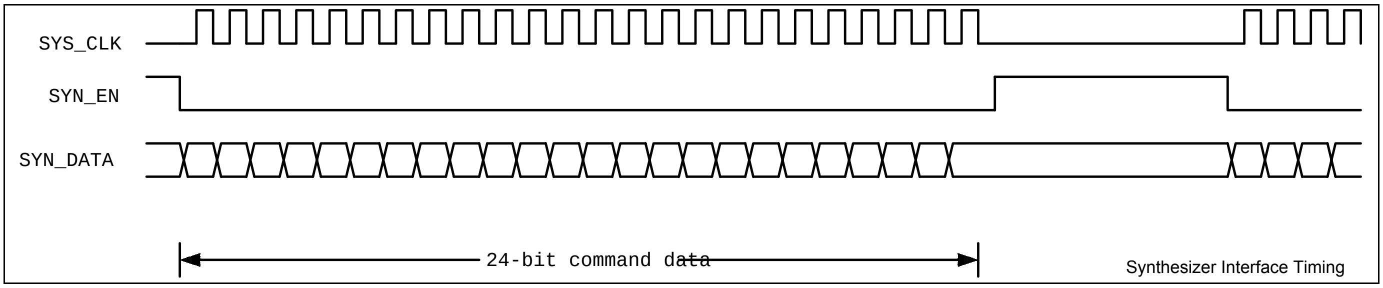


Figure 11. Synthesizer Interface Timing Diagram

Encoder

The Encoder converts analog speech signals from the handset microphone into digital samples for processing. The digitized samples are sent to the BP over the Codec Interface.

The Encoder block is comprised of:

- Input Buffer/Programmable Gain Amplifier (PGA)
- Low Pass Filters
- Σ–Δ ADC
- Digital Filters

The Encoder has two inputs:

- MIC_I+/-
- LINE_I+/-

Only one input can be selected at a time. The inputs are time-multiplexed on the anti-aliasing front stage. Inputs MIC_I+/- and LINE_I+/- can be either single-ended or differential. The encoder analog section has a gain programmability from -4 dB to 40 dB in 1 dB increments, which is distributed between the Anti-Aliasing Filter (AAF) and the ADC. Bit gain settings are performed by register 105h.

Differential Input Mode. The microphone signal is AC-coupled into MIC_IN+ and MIC_IN- pins, which are DC self-biased. To bias the microphone, a low-noise 2.2 V ± 50 mV, MIC_BIAS voltage source is provided by the main reference of the MSD, see Figure 12.

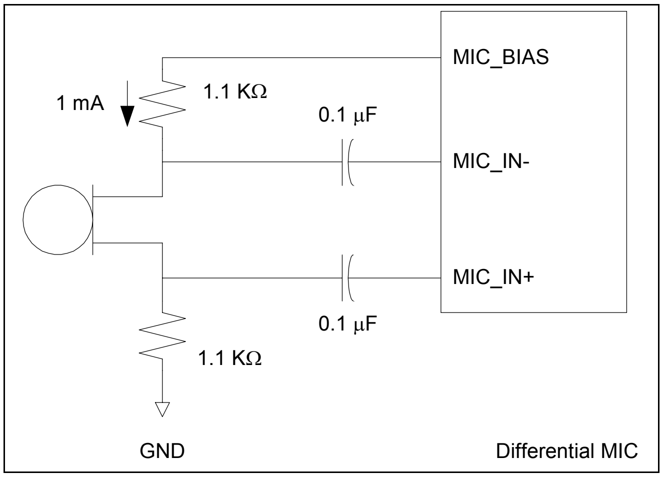


Figure 12. Differential MIC

Single-ended Configuration. The microphone is connected to MIC_IN+; while MIC_IN- is connected to GND with a 100 nF capacitor, see Figure 13. In this mode, the input stage provides a single-ended to differential conversion function.

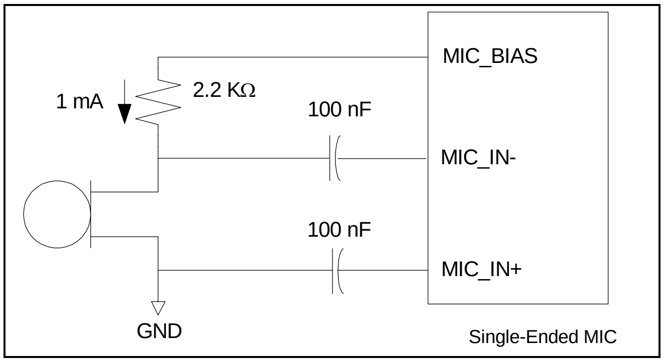


Figure 13. Single-Ended MIC

In a similar way, LINE_I+ and LINE_I- pins are self-biased. In the single-ended configuration mode, the line input is fed through pin LINE_I+, when LINE_I- is connected to GND with a 100 nF capacitor.

The anti-aliasing low pass filter removes the unwanted frequency components from the input signal. The 3 dB cutoff frequency of each filter is typically 100 kHz. The ΣΔADC and internal digital filters convert the input analog signal to 16-bit digital samples at an 8.0 kHz rate. Register 105h is used to control encoder operation.

Decoder

The MSD Decoder receives digital samples over the Codec Interface, and converts the samples to an analog signal. This signal is output from the MSD on one of the two analog outputs. The output signal is used to drive an audio transducer such as the handset speaker.

The Decoder consists of the following devices:

- Digital Filter
- ΣΔDAC
- Low Pass Filter
- Output Buffers

The digital filter in the decoder filters the digitized samples and generates a 1-bit serial data stream. The digital filter receives samples from the BP over the Codec serial interface. The input samples to the filter are 16-bit, two's complement words. The input sample rate is 8 ksps. The output of the digital sigma-delta modulator is a 1-bit serial data stream that is used as the input to DAC. The decoder low pass filter is a reconstruction filter that smoothes the output signal from the DAC.

The Decoder path has two output drivers:

- SPK+ / SPK-
- Driver LINE_O+/-

Both output drivers can operate simultaneously, and can drive a 32 Ω differential load with distortion better than -58 dB at 2.7
VPOWER supply. Each driver has one set of gain control bits that can be set independently. Driver gain is controlled by control-bits linegn[3:0] or Spkgs[3:0] in the decoder control register for line or speaker output respectively. Register 106h is used to control decoder operation.

Codec Interface

The Codec Interface is a four-wire serial interface that is designed to interface between the MSD and the Baseband Processor (BP). The interface is a high speed, synchronous, full duplex, serial communications link. The interface is connected to the MSD Voiceband Codec. The interface signals are as follows:

- CODEC_CLK. 4 MHz interface clock output.
- CODEC_RATE. 8 kHz framing signal output.
- ENCODER_DATA. Serial data output. The bit rate is the same as the CODEC_CLK rate (4 Mbps). The word rate is the same as the CODEC_RATE signal (8 kwps). Words are 16-bits wide.
- DECODER_DATA. Serial data input. The bit rate is the same as the CODEC_CLK rate (4 Mbps). The word rate is the same as the CODEC_RATE signal (8 kwps). Words are 16-bits wide.

During a voice call, the following occurs over the Codec interface:

1. Digitized audio samples are received from the BP over the Codec Interface. The Decoder converts digitized

samples to an analog signal, which is used to drive the handset speaker or the Audio Line Out signal.

2. The Encoder converts the analog signal from the handset MIC_IN+/- or LINE_I+/- input into digital samples. The samples are sent from the MSD to the BP over the Codec Interface.

Figure 14 shows the MSD Codec Interface timing diagram.

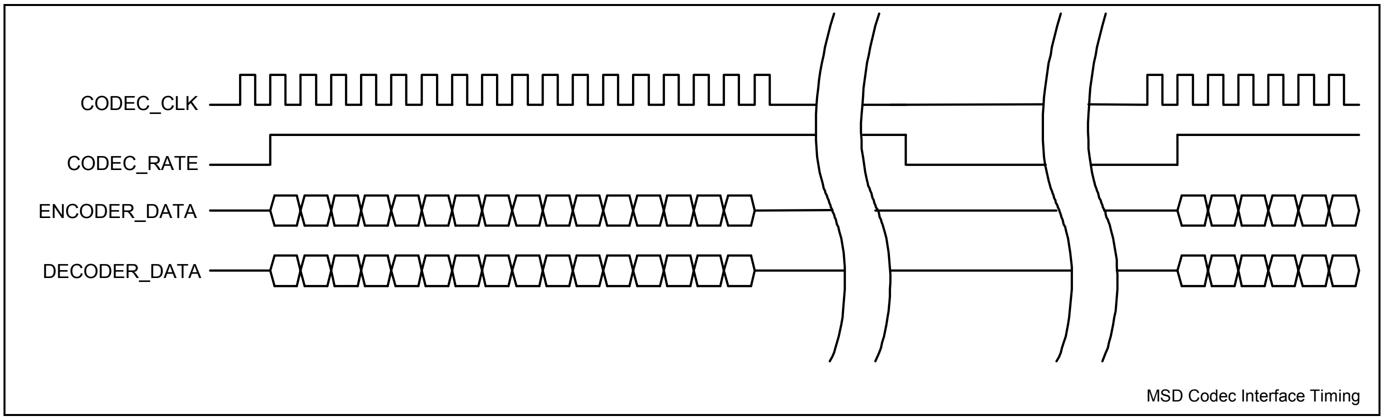


Figure 14. MSD Codec Interface Timing Diagram

Auxiliary ADC

The Auxiliary ADC is a general purpose 8-bit ADC that is used for monitoring external system signals, for example, handset battery voltage.

Each time the Auxiliary ADC is strobed, the 8-bit two's-complement result is placed in bits 15-8 of the RXST1 register. The ADC is strobed whenever bit 15 output from the IFS transitions from 0 to 1. The ADC is read by using the RXST1 (14Bh) register and ADC control register, 120h.

Auxiliary ADC Registers. The Auxiliary ADC register (14Bh) stores the ADC 8-bit output. The ADC value is reported by Bit 15-8 ADC input 2 and Bits 7-0 for ADC input 1. The control of ADC is provided in register (120h) in which gains before ADC is controlled by ADCGN Bit 4-3 as 0, 12, 24 dB. ADC source selection is accomplished by using Bit 9-5. MIC_BIAS is controlled by bit 10, and ADC output type (signed and unsigned) can be selected using Bit 11.

Input to the ADC can be selected using the AUXADC Register (120h) by selecting ADC-select (9-5) 0000.

Temperature Sensor

The reference block includes a temperature sensor. It generates a current proportional to absolute temperature that is converted into a voltage. Table 2 lists the temperature sensor registers. Refer to register 11Bh. The temperature sensor reading is performed using the ADC.

Table 2. Temperature Sensor Registers

Signal Name	Function	Description
tsense_en	Temperature sensor enable	High: block enabled. Low: block disabled temp_sens_out=0 V
temp_sens_out	Temperature sensor output	Voltage range: [0.42 V; 2.26 V] Step: 16.6 mV/°C Tempmax: +80°C → 0.42 V Tempmin: -30°C → 2.26 V @ +25°C → 1.35 V

General Purpose Output (GPO)

The GPO block circuit allows any of the dynamic signals from the IFS Store, the two-band signals (Hiband and Loband), from the Tune Store, and the static register bit AuxAnt, to be routed to any of the 12 available GPOs. In addition, every signal has the capability to invert its output, by setting a register bit.

The circuit can be considered as a cross point switch with full programmability.

The single circuit for one GPO is divided in components:

- IFS Control
- Aux Antenna Control
- Band Control

The single outputs of these three blocks are ANDed together.

IFS Control

The IFS Control either multiplexes several IFS-signals together or routes one specific IFS signal to the output of this sub-block. The control bits of registers GPO0 to GPO11 allow programmability in accordance with GPO output bits 0 - 9. The IFS control truth table is listed in Table 3.

Auxiliary Antenna Control

The Auxiliary Antenna Control portion allows routing (with or without inversion) the auxiliary antenna signal to the output of the sub-block. The control bits of registers GPO0 to GPO11 allow programmability of GPO output register bits 10-11. The auxiliary output bits are listed in Table 4.

Band Control

The Band Control portion allows routing the two-band signals (Hiband and Loband) to the output of this sub-block. The control bits of the registers GPO0-GPO11 use GPO output register bits 12-14. Band control output bits are listed in Table 5.

Inversion Control

The three outputs of the sub-blocks IFS-Control, AUX-control and BAND-control are ANDed together and fed to an inversion block, before it gets routed to the GPO pad using GPO output bit 15.

Table 3. IFS Control Truth Table

IFS[0]	Control[9:1]	IFS[0],…,IFS[13]	IFS-Output
0	V	X	Or of enabled terms
1	X	X	1

Table 4. Auxiliary Antenna Control Bits

AUX[10]	AuxAnt[11]	MASEN[1]	AUX-Output
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	X	X	1

Table 5. Band Control Output

BAND[14]	HiBand[13]	LoBand[12]	TUNE[0]	TUNE[1]	BAND-Output
0	0	0	X	X	1
0	0	1	X	0	0
0	0	1	X	1	1
0	1	0	0	X	0
0	1	0	1	X	1
0	1	1	0	0	0
0	1	1	1	X	1
0	1	1	X	1	1
1	0	0	0	X	0
1	0	0	X	0	0
1	0	0	1	1	1
1	0	1	X	0	0
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	X	0
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	1

Power Management

Power-Up Sequencing

Power-up is initiated by pulling the PWR_KEY_L, the ALARM, or the DTR line below Vil_{max}, or pulling the PWR_KEY_H line above Vih_{min}. Also, connecting an external power source for the charger (VCHARGE) initiates the normal power-up sequence. This applies power to the internal circuitry. VCORE and VIO rise and the power-up sequence will commence. POR is forced low until VIO is above 92 percent of the steady-state value.

The POR circuit monitors the VIO regulator output voltage. When the output voltage of the VIO regulator drops eight percent of nominal value, the POR_OUT is forced low and the MSD shuts down. A falling edge on MSD_RESET also powers off the MSD.

Voltage Regulation

Electrical specifications for the voltage regulators are listed in the tables at the end of this Data Sheet.

Reference Voltage Generation

The reference block provides voltage and current references to the CX20524. A bandgap generates a voltage of 1.2 V. The
1.2 V is also used to generate a reference current of 40 µA through the 30 kΩ off-chip RBIAS resistor. This reference current is divided down and mirrored to provide current references to the different blocks. To ensure low noise density on the current source, the bandgap voltage is filtered by a first order low-pass filter. Moreover, an additional filter formed by a 30 kΩ internal resistor and a 0.1 µF external capacitor (on pin MIC_CAP) is used before the MIC_BIAS buffer to meet the noise specification for this reference. The settling time for the voltage references is less than 500 µs with the exception of MIC_BIAS, which requires about 10 ms.

Regulators for Internal Use

The GSM Mixed Signal Device contains the Low Drop Out (LDO) Regulators necessary to support a multi-band GSM/GPRS handset. The internal regulators provide 2.825 V (typical) output voltage. The internal LDO’s are not recommended for system use. Its main purpose is to provide a stable supply and isolation to different sections of the MSD.

There are five regulators that provide power to the MSD's internal blocks; VD1 and VD2 pins are used for digital blocks while the remaining three regulators are used for analog blocks.

The regulator generating the digital supplies is enabled at all times, while all analog regulators can be powered down using register 131h. The supply VD1 is used to provide power to the logic controlling the enable signals for analog regulators. VD1 is also used to provide power to the bandgap reference, which must to be ON in case any of the analog regulators are active.

VAUX1, VAUX2, VAUX3, and VAUX4 are reserved for future use. However, they must be decoupled to ground with a 100 nF capacitor.

Each LDO requires a 100 nF external ceramic capacitor, to ensure stability of the regulator and provide low impedance at high-frequency.

Regulators for External Use

All regulators that are required to support the Skyworks Pegasus chipset are contained in the MSD. There are six regulator for external use. The VCORE, VIO, and VSIM regulators are optimized for low ground current (50 µA each). The regulators are controlled independently via the serial port or the three enable pins (EN_1, EN_2, and EN_3).

VCORE and VRTC Voltage Select Pins

Refer to Table 6.The VCORE and VRTC output voltages are selectable using the VSEL0 and VSEL1 pins. The pins are either tied to ground or left open. The inputs are internally pulled up to either BACKUP or VPOWER.

Table 6. VCORE and VRTC Voltage Select Pins

VSEL1	VSEL0	VCORE	VRTC
Ground	Ground	1.2	1.2
Ground	Open	1.7	1.7
Open	Ground	2.4	2.4
Open	Open	2.8	2.4

Bandgap and Regulator Adjustability

To maximize flexibility and minimize power consumption in active and standby modes, one of the voltage references (bandgap) can be adjusted via the register OAh that is accessible through the low speed asynchronous serial port. The system voltage regulator's output can be adjusted dynamically using VOCRE, VRF, VTIC, and VUHF. Furthermore, the output voltage range of VCORE and VRTC are selectable using two dual function pins (VSEL0 and VSEL1). Possible voltage ranges are: 1.2 V, 1.7 V, 2.4 V and 2.8 V.

Figure 15 is an example of a voltage adjustment scenario. The first bandgap is tuned so all regulators are within ± 0.8% of nominal values. After tuning the VCORE voltage, it can be increased up to +7.2% for a high speed DSP application. In addition it can be made -6.3% lower than nominal for sleep duration. During sleep, the bandgap can be reduced to a minimal value to provide -8.5% lower voltage. On wakeup, both bandgap and VCORE voltages can be returned to nominal values. Similar examples can be made for VRF, VUHF, VTIC voltages. In changing the voltages based on the operating state of the handset, be aware of the physical limitations of each device, so that system does not hang up when voltages are changed.

Battery Back-up and RTC System

A low current pre-regulator receives input from VPOWER and regulates it down to 3.3 V.

The battery backup can be either a primary lithium cell or a super-capacitor. This component maintains a charge in the event that the main battery pack is removed and the Real Time Clock (RTC) circuit needs to keep time. A low voltage regulator takes the back-up component voltage and regulates it down to one of three possible voltages (1.2 V, 1.7 V, or 2.4 V). The V_{RTC} output voltage is selected by using the VSEL0 and VSEL1 pins.

Figure 16 shows the RTC battery diagram. Battery back-up and RTC electrical specifications are listed at the end of this document.

When the battery voltage (VBATTERY) at ISN pin decays within
± 10 mV of the backup voltage (VBACKUP) battery/capacitor (VBATTERY – VBACKUP comparator hystersis) the circuit enters into backup mode in which pre-regulator is turned off to prevent reverse discharge of the backup battery or capacitor. Once in this mode the RTC regulator operates exclusively from the backup voltage (battery/capacitor). When VBATTERY increases by 205 ± 60 mV above the VBackup pre-regulator turns on and

resumes powering the RTC regulator and also charging the back-up component (battery/capacitor).

Battery Charger

The control circuit (required for the battery charger) is located inside the CX20524 MSD. The Host BP software is required to complete the charger function.

Fail-Safe Mode

Charger implementation is similar to a voltage regulator using an external pass transistor. After the DAC value is set, it enables current to flow and charge the battery. The fail-safe mode is achieved by utilizing a voltage feedback to offset the control signal to the external pass transistor gate driver circuit. As the battery voltage increases, the current will decay.

Various tasks executed during the charging cycle are under the control of the software.

Refer to the *Sample Battery Charging Application User Guide*, 101946B for detailed information about charging batteries.

Charging the Battery

Figure 17 shows a typical charging circuit for the MSD. An internal multiplexer controls the output to MUX_OUT. Inputs are BAT_PK_IN (battery pack resistor), Current Sense, VCHARGE, VBATTERY, DAC VOLTAGE. The output can be connected to AUXADC+ to measure different parameters.

The DAC controls the gate voltage for external mosfet that controls the Current/ Voltage output to VBATTERY. The maximum current used for charging is limited by the package thermal characteristics.

A charging current profile is shown in Figure 18. Current in shaded area is not recommended for internal sense resistor during charging. For higher charging currents connect an external 0.10 • sense resistor between ISN and ISP in parallel with the internal R_{Sense}. This will provide twice the charging current capacity compared to internal $R_{Sense.}$

Operating when the Battery is Dead or not Present

There are occasions when the battery pack will have been discharged below the handset normal cutoff voltage. In those instances, the CX20524 allows the system to be powered from VPOWER, instead of VBATTERY. Since the MSD is powered from VPOWER, most of the system operates normally, even if the battery pack is removed.

Also, the MSD is able to operate normally, even if the battery pack is not present. The software recognizes that the battery pack is not present by attempting to measure the battery pack resistor or battery voltage.

SIM Interface

In a GSM handset application, the handset interfaces to a SIM card, which contains subscriber-specific information. Depending on the SIM card, a supply voltage of 1.8 V or 2.8 V is required.

Refer to Figure 19.The output voltage selector switch is controlled by bit 6 of the Power Management Control Register. When the handset powers up, the system controller must first determine whether the SIM card being used is a 1.8 V or 2.8 V card. The default value of bit 6 is set for a 2.8 V output. The controller must write a “0” to bit 6 of the Power Management Control Register to select a 1.8 V output.

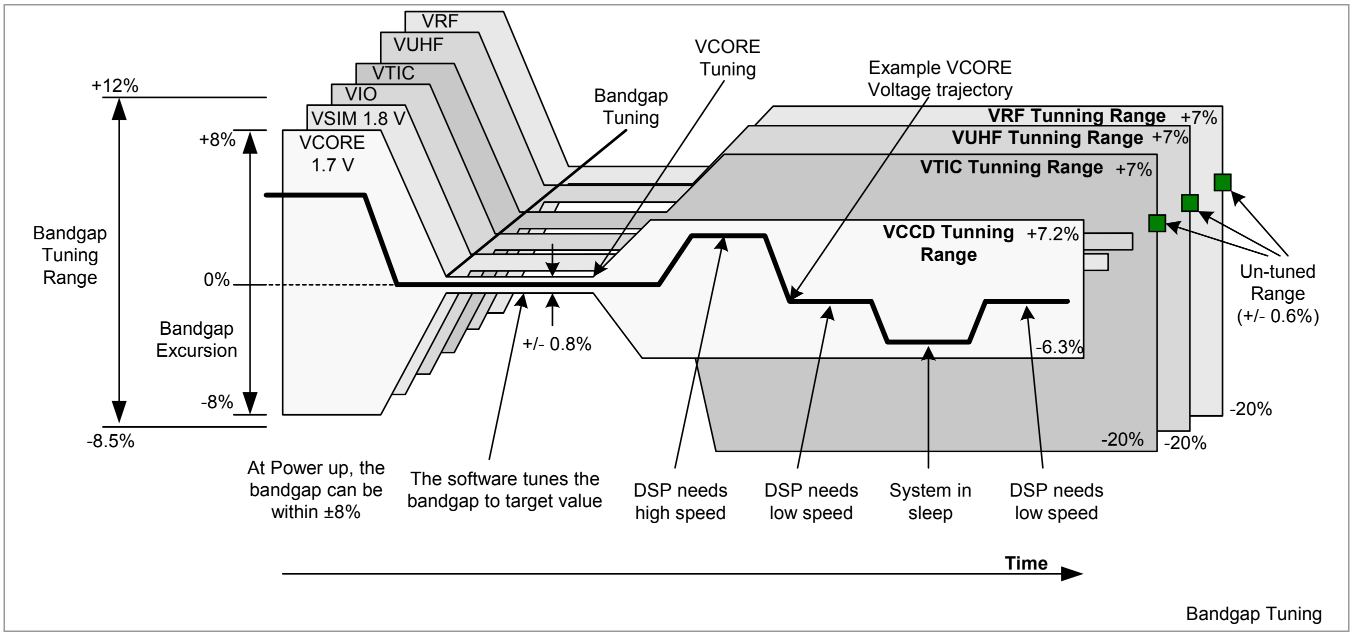


Figure 15. Bandgap Tuning Example

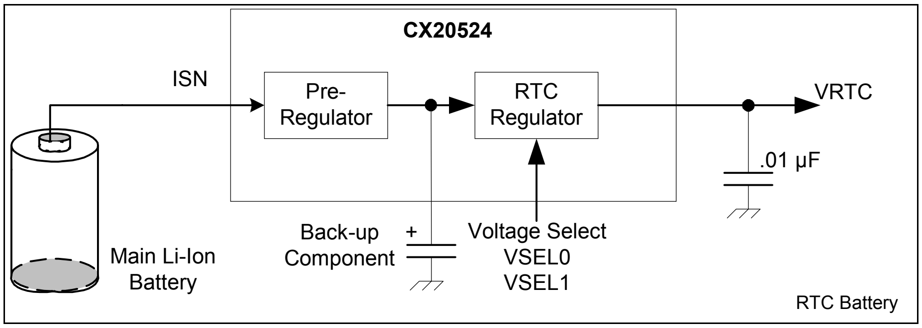


Figure 16. RTC Battery

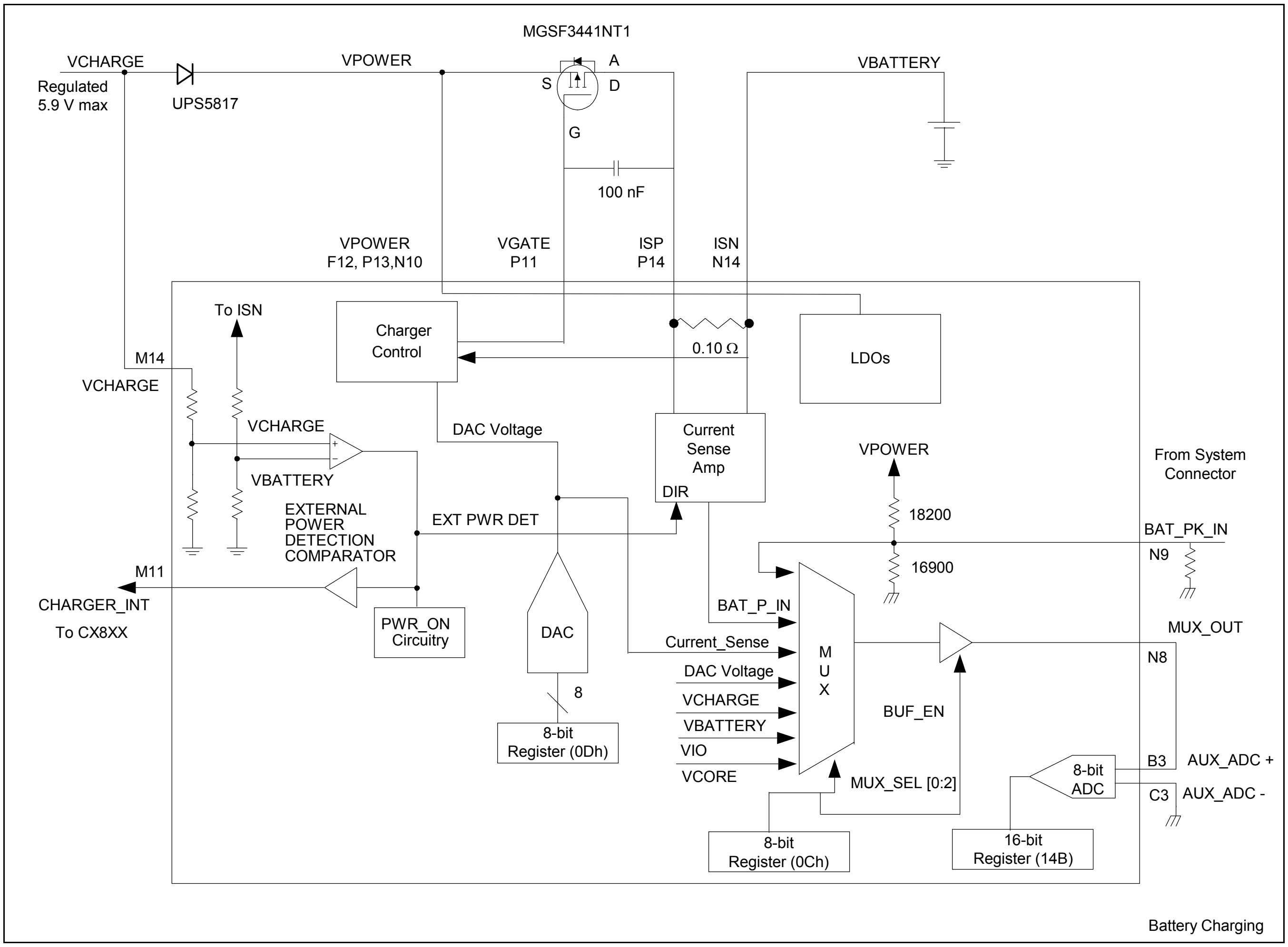


Figure 17. MSD Battery Charging

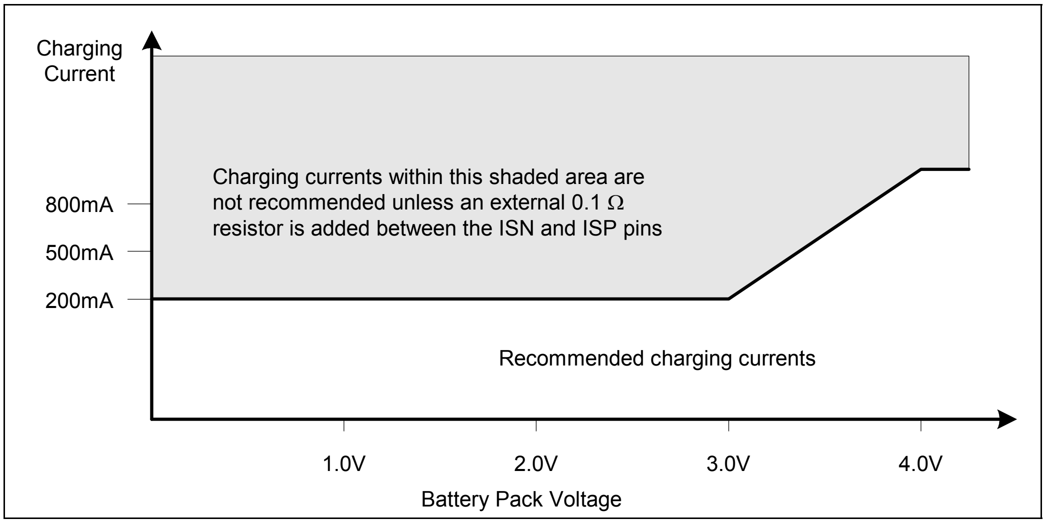


Figure 18. Maximum Charging Current for Different Battery Voltages

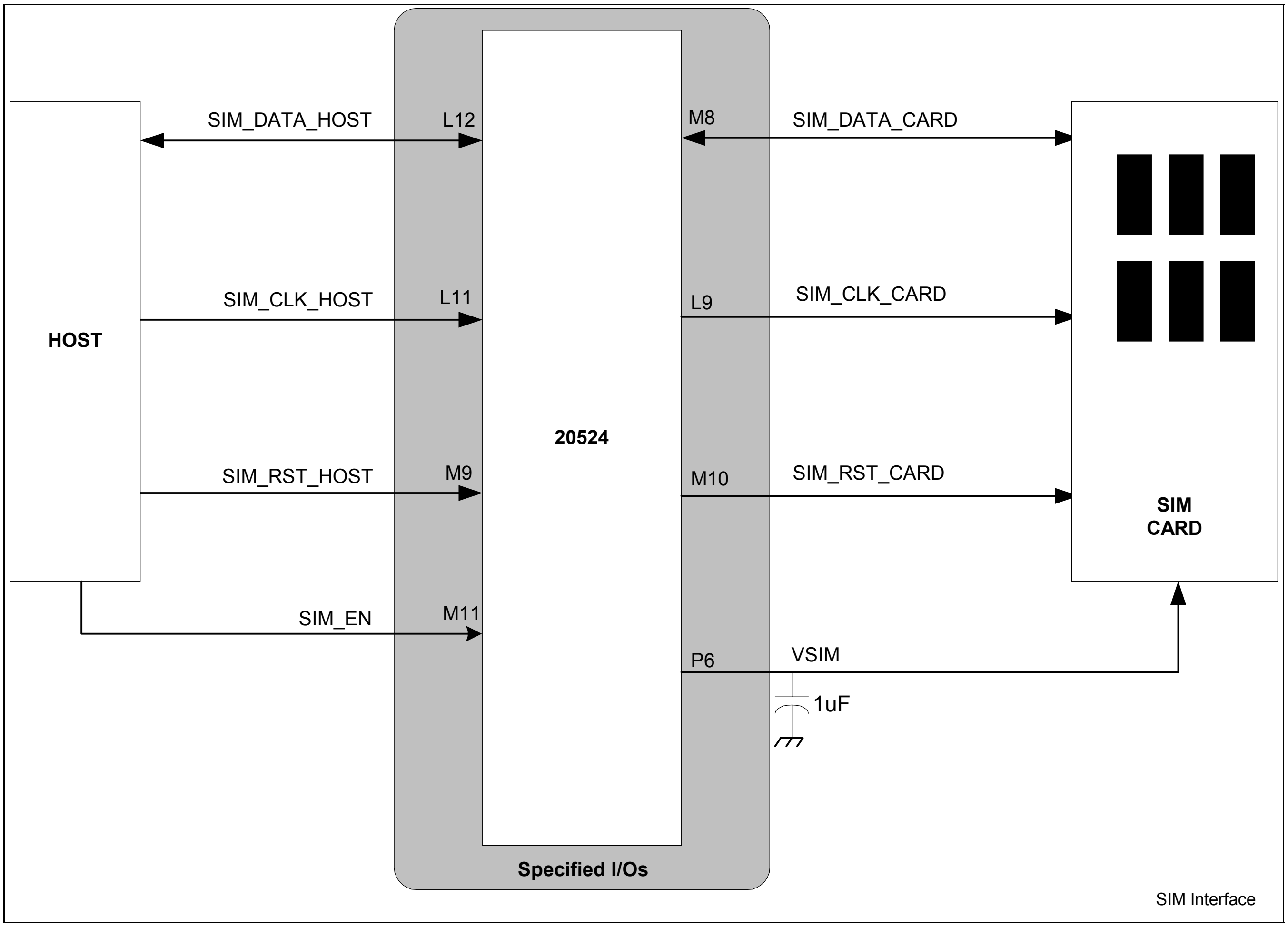


Figure 19. SIM Interface

Low Speed Asynchronous Serial Port

Communication Interface

The SERIAL_DATA is a bi-directional line, connected to the positive supply voltage via a pull-up resistor. When the bus is free, both the SERIAL_DATA and SERIAL_CLOCK lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. Data can be transferred at a rate up to 100 kbit/s. As defined in the specification, the levels of the logical ‘0’ (LOW) and ‘1’ (HIGH) are fixed. The data on the SERIAL_DATA line must be stable during the HIGH period of the SERIAL_CLOCK. The HIGH or LOW state of the SERIAL_DATA line can only change when the clock signal on the SERIAL_CLOCK line is LOW as shown in Figure 20.

Within the communication procedure of the serial bus, unique situations arise which are defined as START and STOP conditions, see Figure 21. A HIGH to LOW transition on the SERIAL_DATA line while SERIAL_CLOCK is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SERIAL_DATA line while SERIAL_CLOCK is HIGH defines a STOP condition. The master always generates START and STOP conditions. The bus is considered to be busy after the START condition.

Serial data transfer on a low speed asynchronous serial bust is byte-oriented. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first.

Data transfer with acknowledges is obligatory. The master generates the acknowledge-related clock pulse. The transmitter releases the SERIAL_DATA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SERIAL_DATA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse. Usually, a receiver which has been addressed is obliged to generate acknowledge after each byte has been received. The master can then generate a STOP condition to abort the transfer.

Communication sessions between the BP (Master) and the MSD (Slave) are always initiated via the start condition followed by, the device address (limited to 7-bits plus one R/W bit), and the register address byte. Refer to Figure 22. In the single register access, the third byte does represent the data information written or read by the Master. In the sequential mode, the register address is the starting register, and then up to 16 bytes of data can be read or written from/to the MSD. Writing more than 16 bytes will effectively over-write the previous information. The address is 100100x. See Figure 23.

Watch Dog Timer

The watch dog timer circuit (Figure 24) initiates a system reset when there is no interaction between the MSD and BP. If the BP fails to load the burst store for two consecutive frames (where transmission should occur), the MSD generates a reset signal to the BP and the rest of the system. The MSP similarly generates a system reset if the BP has not accessed any MSD control registers for two consecutive cycles of an active intra-frame sequencer.

The watch dog timer is enabled by setting bit (WDEn) bit 5 13Fh register (MASEn). For testing purposes and to allow the BP to force a reset, a system reset is generated with the Sys_Reset bit, bit 0, 13Eh register (Master XO register). This condition forces a reset only if the watch dog timer is enabled.

The watch dog is enabled by setting bit WDEn. Once set, wd_clk starts. In Figure 24, wd_clk is running at 4.3 MHz. IFS is enabled by setting bits 15-14 (IFSEn), 13Fh register (MASEn). When the IFS duration and address count starts (1st data frame), the internal loop1 logic goes high. An access to the MSD control register resets the internal loop1 and loop2 signals and starts the watch dog time again. When both loop1 and loop2 logics are high, the internal wd_reset pulse is generated, causing RESET_B to go low for 60 µsec. If IFSEn is enabled, and no action is taken, the watch dog reset starts in 112 µsec. If IFSEn is enabled, the next instruction to IFS address 000h, bit 15, is set then the watch dog reset starts in 2 µsec. Since IFS add count is relatively short, the IFS address count will jump back to the zero address in the first store.

Sleep Mode

Refer to Figure 6 for the following process flow:

1. If the BP determines that there are no processing requirements, it directs the MSD to go to sleep.
2. The BP stops the MSD and puts it into a safe state. Additionally, it informs the MSD what to do when a CLK_EN signal is taken low. There are three options for BP:
   - Shut off the 3.9 MHz buffer but let the internal timing chain run from the 19.5 MHz oscillator
   - Shut off the 3.9 MHz and the internal timing chain but keep the 19.5 MHz oscillator running
   - Shut off the 3.9 MHz and the timing chain and the 19.5 MHz oscillator

3. The MSD retains this information and waits for the CLK_EN signal to go low, before shutting anything down.

4. The BP may write to the MSD Registers, at any time, to power down the analog regulators (including XTAL regulator). If internal regulators are not powered down, the analog and oscillator supplies stay on continuously no matter what the state of the CLK_EN signal. If they are powered down, it will turn off the analog and oscillator supplies when CLK_EN goes low.

5. BP takes the CLK_EN and MSD_SLEEP signals low. When the CLK_EN signal goes low, it is sensed by the MSD. The MSD shuts off its sections, working backwards from the 3.9 MHz buffer. Optimally, the MSD puts itself into a safe state and then shuts off the 19.5 MHz oscillator.

6. The MSD will also monitor the MSD_SLEEP signal. If this signal is low it will turn-off VCORE, VSIM, VIO regulators.

7. The device is now in a minimum power Sleep State.

Waking Up from Sleep Mode

To wake up from sleep mode:

1. The MSD responds to the CLK_EN/MSD_SLEEP going high by immediately turning on regulators VCORE, VIO and the internal analog regulators (if they had been turned off during the sleep period). These regulators must be turned on immediately without any delay.

2. The MSD responds to the CLK_EN going high by enabling the oscillator, the timing chain, and the 3.9 MHz output buffer. This ensures all sections start up properly. Any blocks not turned off should be stable and the MSD does not need to re-initialize them. Conversely, if the MSD has only shut down the 3.9 MHz buffer (timing chain and oscillator left enabled) then the 3.9 MHz clock outputs immediately.

The maximum sleep and OFF mode currents are listed in Table 7.

Table 7. Sleep and Off Modes

Mode	Max Current (µA)
Sleep Mode (VCORE, VIO ON)	200
OFF Mode	45

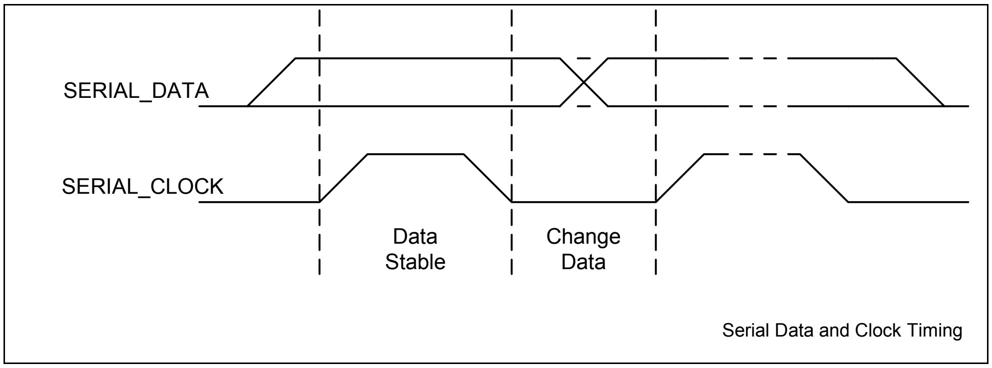


Figure 20. Serial Data and Clock Timing

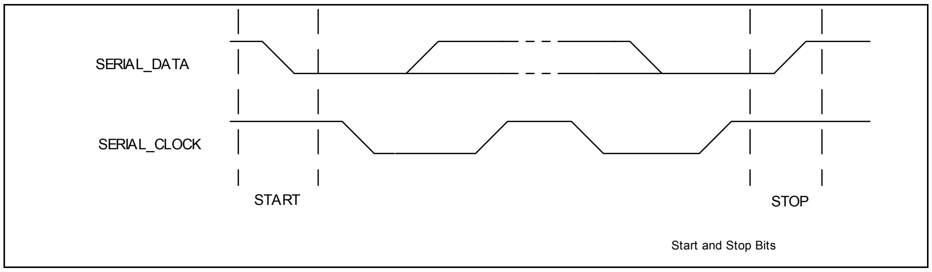


Figure 21. Start and Stop Bits

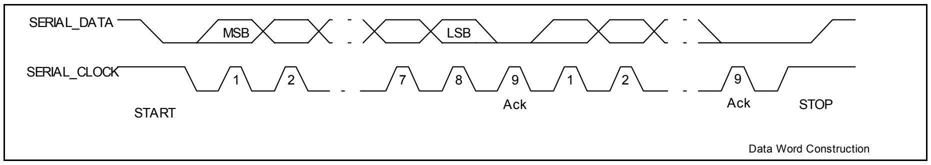
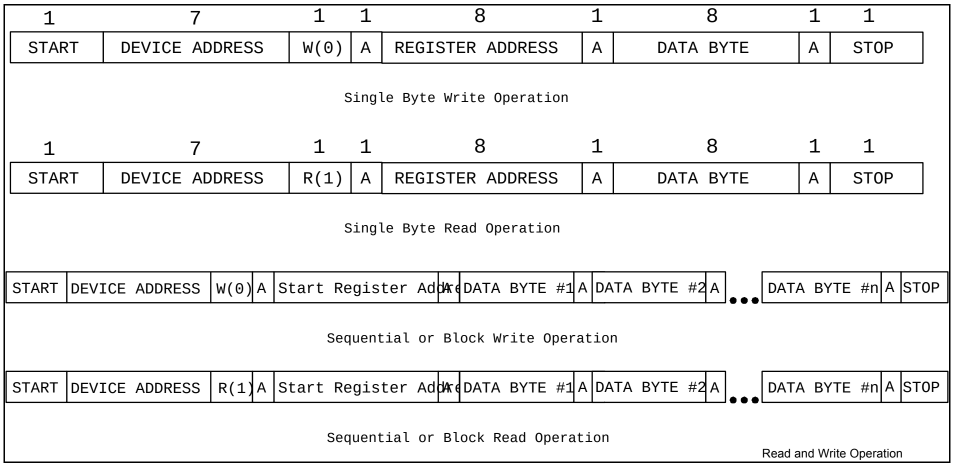


Figure 22. Data Word Construction



1	7	1	1	8	1	8	1	1
START	DEVICE ADDRESS	W(0)	A	REGISTER ADDRESS	A	DATA BYTE	A	STOP

Single Byte Write Operation

1	7	1	1	8	1	8	1	1
START	DEVICE ADDRESS	R(1)	A	REGISTER ADDRESS	A	DATA BYTE	A	STOP

Single Byte Read Operation

START	DEVICE ADDRESS	W(0)	A	Start Register Add	A	DATA BYTE #1	A	DATA BYTE #2	A	•••	DATA BYTE #n	A	STOP

Sequential or Block Write Operation

START	DEVICE ADDRESS	R(1)	A	Start Register Add	A	DATA BYTE #1	A	DATA BYTE #2	A	•••	DATA BYTE #n	A	STOP

Sequential or Block Read Operation

Figure 23. Sequential or Block Read/Write for Low Speed Asynchronous Serial Port

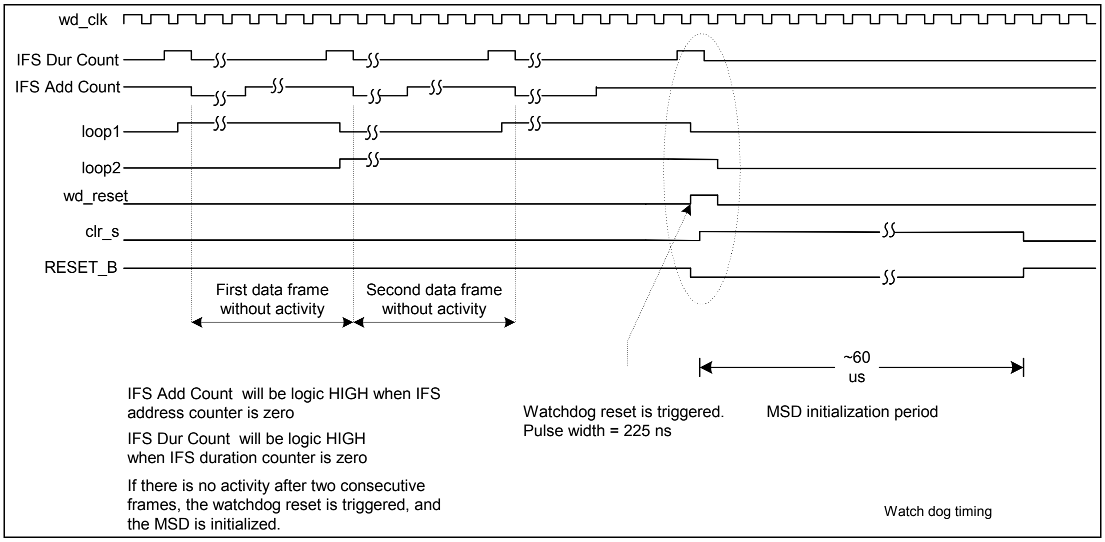


Figure 24. Watch Dog Timing

Device and Register Addresses

The MSD address is 1001000.

Register Bank Description

This section describes the register table of the device, which can be programmed over the four-control interface and using two-wire serial interface.

Table 8 lists the registers (which are 16-bit length) that are programmed using the four-wire control interface and grouped into the following:

- Store register (address 000h - 0FFh)
- Control register (address 100h - 13Fh)
- Monitor register (address 140h - 14Fh)

They are used to control the receiver, transmitter, transmit power, timing generation and control, synthesizer interface voiceband codec, auxiliary ADC, and internal voltage regulators.

The store registers are represented in RAM cells. There are four stores inside the device, which are called Intra-frame Sequencer Store, Ramp Store, Tune Store, and Burst Store. The stores are able to generate dynamic signals (slot enable controls).

The control registers store static information, which control all the different analog and digital blocks. Most of them are system control bits. However, certain bits are only used for device level testing.

The monitor registers are read only registers, which allow the baseband processor to read status bits from the device.

For a description of these registers, refer to Table 10 through Table 42.

The power management registers are programmed using two-wire serial bus and are 8-bit length. They are listed from address space 00h - 0Fh. Refer to Table 9.

These registers are used to control the external voltage regulators, device power-up, power down, battery charge and monitor control, and SIM card interface control.

For a description of these registers, refer to Table 43 through Table 54.

Table 8. 16-Bit Register Addresses

Addr.	Name	Function	Read/Write	Default Value (Hex)
000-07F	Intra-Frame Sequencer	RAM for Intra-Frame Sequencer state machine	R/W	0000
080-0BF	Ramp Store	RAM for transmitter power ramping profile	R/W	
0C0-0DF	Synthesizer Sequencer	RAM for Synthesizer Sequencer state machine	R/W	
0E0	Burst Store RAM	RAM for storing one burst of data bits to be modulated	R/W	
100	Tx Offset	Adjusts I/Q transmit channel DC offset voltage	R/W	
101	TX I/Q Control	Adjusts I/Q transmit channel gain imbalance	R/W	
102	CCXOO	Crystal oscillator output coarse tune	R/W	
103	CCXOI	Crystal oscillator input coarse and fine tune	R/W	
104	Reserved	Reserved	R	
105	Encoder Control	Controls the voiceband encoder operation	R/W	
106	Decoder Control	Controls the voiceband decoder operation	R/W	
107	RXCTL	RX control register	R/W	
108	TXCTL	TX control register	R/W	
109-10D	Reserved	Reserved	R	
10E-119	GPO	GPO control registers	R/W	
11A	Reserved	Reserved	R	
11B	MSCCTL	Miscellaneous control register	R/W	
11C-11F	Reserved	Reserved	R	
120	ADC Control	ADC control registers	R/W	
121-125	Reserved	Reserved	R	
126-12C	Test	Codec, Rx, Tx, Test registers	R/W	
12D	RXPD	Receiver power down register	R/W	
12E	TXPD1	Transmit power down register 1	R/W	
12F	TXPD2	Transmit power down register 2	R/W	
130	Reserved	Reserved	R/W	
131	REGPD	Internal regulators control	R/W	
132-13D	Reserved	Reserved	R	
13E	MASXO	Master XO register	R/W	
13F	MASEn	Master enable register	R/W	
140-141	Reserved	Reserved	R	
142	GPO Mon	Monitors GPO status	R	
143-14A	Reserved	Reserved	R	
14B	RXST1	ADC value read register	R	
14C	Reserved	Reserved	R	
14D	RXST2	Receiver status register	R	
14E	Reserved	Reserved	R	

Table 9. 8-Bit Registers Addresses

Addr.	Name	Function	Read/Write	Default Value (Hex)
00h	Reserved	Reserved	-	00
01h	VRF tuning & Control	Tuning and control for VRF regulator	R/W	FB
02h	Override control	Override pin control and register	R/W	80
03h	PM Control	Power management control register	R/W	CE
04h	LDO VRF	Enable control for VRF	R/W	01
05h	LDO VTIC	Enable control for VTIC	R/W	02
06h	LDO VUHF	Enable control for VUHF	R/W	01
07h	Reserved	Reserved	-	FF
08h	Power up Status	Power up status register	R	00 to 0F
09h	VTIC tuning & Control	Tuning and control for VTIC register	R/W	FB
0Ah	Bandgap Tuning	Bandgap tuning register	R/W	07
0Bh	VUHF tuning & Control	Tuning and control for VUHF register	R/W	FB
0Ch	MUX Control	Mux out control register	R/W	02
0Dh	DAC Value	DAC value input register for VGATE	R/W	00
0Eh	Reserved	Reserved	-	00
0Fh	Reserved	Reserved	-	00

Table 10. IFS: Intra Frame Sequencer Store, Register 1

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
000h, 002h-07Fh	DUR	[14:0]	Number of 2 MHz-clock cycles for next odd IFS-register-address	0…0
	RESET	[15]	Reset state sequence: jumps back to address zero	0

Table 11. IFS: Intra Frame Sequencer Store, Register 2

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value

001h, 002h-07Fh	F_Rate	[0]	Provide frame timing and wakeup call to DSP	0
	Reserved	[1]	Reserved	0
	SubSeqEn	[2]	Enable Ramp & Tune sequencers	0
	Tune	[3]	Invoke Tuning Sequence	0
	Reserved	[4:5]	Reserved	00
	RxEn1	[6]	Enable (power) external Rx chain	0
	IRxEN	[7]	Internal Rx Enable	0
	Tx_Rx	[8]	Select Aux synthesizer center frequency for Tx Vs. Rx 0 = Rx is selected 1 = Tx is selected	0
	RxSlot	[9]	Identify Rx Vs. Monitor slot	0
	AntEn	[10]	Enable selected antenna via RxEn0 or TxEn0	0
	Ramp	[11]	Invoke Ramp sequence	0
	TxEn2	[12]	Enable power for PAC	0
	TxEn1	[13]	Control of external Tx Enable	0
	ItxEn	[14]	Internal Tx Enable	0
	CalStrobe	[15]	Leading edge strobes calibration ADC	0

Table 12. Ramp Store Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
080h-0BFh	DUR	[4:0]	Number of 2 MHz-clock cycles for duration of PAC output-value	0…0
	Reserved	[5]	Reserved	0
	VAL	[15:6]	Ramp store output value	0…0

Table 13. TUNE: Tune Store, for Synthesizer Register 1

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value

0C0h, 0C2- 0DFh	SynCmd	[14:0]	MSB's of Synthesizer Commands	0…0
	RxPgaGn	[9:8]	Gain Control of Rx PGA3 00 = 0 dB 01 = 6 dB 10 = 12 dB 11 = 12 dB	0…0
	RxLpfGn	[11:10]	Gain Control of Rx Low pass filter 00 = 0 dB 01 = 6 dB 10 = 12 dB 11 = N/A	0…0
	RxGain0	[12]	Gain Control for external PGA in RF-Rx-path	0
	RxGain1	[13]	Gain Control for PGA1 in RF-Rx-path 0 = low gain: -9 dB 1 = high gain: 24 dB	0
	RxGain2	[14]	Gain Control for PGA2 in RF-Rx-path 0 = low gain: 0 dB 1 = high gain: 12 dB	0
	SynthSel	[15]	Chooses between Syn0Rate and Syn1Rate 0 = Activates Syn0Rate (Internal synthesizer mode) 1 = Activates Syn1Rate (External synthesizer mode)	0

Table 14. Band Select Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
0C1h, 0C2- 0DFh	BandSel	[1:0]	Selects between different bands 00 = leave HighBand and LowBand unchanged 01 = clear HighBand and set LowBand 10 = set HighBand and clear LowBand 11 = set both for MidBand	0…0
	LoadGain	[2]	Control for setting gain-bits [14:8] in first tune word 0 = leave unchanged 1 = load new value	0
	LoadIS	[3]	Control for setting IS-bits [5:4] in second tune word 0 = leave unchanged 1 = load new value	0
	RxIS	[4]	Switches I and Q-channel for Rx 0 = normal mode 1 = I and Q-channel are switched	0
	TxIS	[5]	Switches I and Q-channel for Tx 0 = normal mode 1 = I and Q-channel are switched	0
	SynCmd	[15:8]	LSB's of Synthesizer Commands (Bit 7:0)	0…0

Table 15. BURST: Burst Store

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
0E0h-0FFh	DAT	[15:0]	Tx data value	0000h

Table 16. TXOFF: Tx Offset Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
100h	TXQOff	[7:0]	Specify the DC offset compensation for Tx Q channel	00h
	TXIOff	[15:8]	Specify the DC offset compensation for Tx I channel	00h

Table 17. TXIQ: Tx I/Q Control Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th colspan="4">Description (Default = 0000h)</th><th>Default Value</th></tr>
<tr><td rowspan="13">101h</td><td rowspan="9">TxIQ</td><td rowspan="9">[5:1]</td><td colspan="4">Tx I/Q gain balance adjustment</td><td rowspan="9">0…0</td></tr>
<tr><th>Code</th><th>I/Q - 1</th><th>Code</th><th>I/Q - 1</th></tr>
<tr><td>10000</td><td>-7.5%</td><td>00000</td><td>0.5%</td></tr>
<tr><td>10001</td><td>-7.0%</td><td>00001</td><td>1.0%</td></tr>
<tr><td>10010</td><td>-6.5%</td><td>00010</td><td>1.5%</td></tr>
<tr><td>10011</td><td>-6.0%</td><td>…</td><td></td></tr>
<tr><td>…</td><td></td><td>01101</td><td>7.0%</td></tr>
<tr><td>11110</td><td>-0.5%</td><td>01110</td><td>7.5%</td></tr>
<tr><td>11111</td><td>0%</td><td>01111</td><td>0%</td></tr>
<tr><td>TxCmSel</td><td>[6]</td><td colspan="4">Common mode select of Tx path
0 = disable
1 = enable</td><td>0</td></tr>
<tr><td>TxCtfAm</td><td>[7]</td><td colspan="4">Amplitude control of Continuous Time Filter
0 = 0.8 Volt differential peak to peak
1 = 1 Volt differential peak to peak</td><td>0</td></tr>
<tr><td>PhIQ</td><td>[10:14]</td><td colspan="4">Specify the value for TxIq-Phase shift in 2’s complement.</td><td>0…0</td></tr>
<tr><td>PhCByp</td><td>[15]</td><td colspan="4">Bypass of phase correction circuit
0 = normal mode
1 = bypass mode</td><td>0</td></tr>
</table>

Table 18. CCXOO: CCXO Output Control Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
102h	CoarseO	[15:9]	Coarse adjustment for CCXO Output	00h

Table 19. CCXOI: CCXO Input Control Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
103h	Finsel	[8:0]	Fine adjustment for CCXO Input	00h
	Coarsel	[15:9]	Coarse adjustment for CCXO Input	00h

Table 20. ENC: Encoder Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
105h	MicEn	[0]	Enable control of Microphone 0 = disable 1 = enable (Over rule LineIEn)	0
	LineIEn	[1]	Enable control of Input Line 0 = disable 1 = enable	0
	MicGn	[5:2]	Gain control of Mic path (AAF + ADC) 0000 = 0dB 0001 = 3 dB 0010 = 6 dB 0011 = 9 dB 0100 = 12 dB 0101 = 15 dB 0110 = 18 dB 0111 = 21 dB 1000 = 24 dB 1001 = 27 dB 1010 = 30 dB 1011 = 33 dB 1100 = 36 dB 1101 = 39 dB 1110 = 40 dB 1111 = Not defined	0…0
	LineIGn	[9:6]	Gain control of encoder line path (AAF + ADC) 0000 = 0dB (Gain mapping is the same as MicGn) 0001 = 3 dB 0010 = 6 dB 0011 = 9 dB 0100 = 12 dB 0101 = 15 dB 0110 = 18 dB 0111 = 21 dB 1000 = 24 dB 1001 = 27 dB 1010 = 30 dB 1011 = 33 dB 1100 = 36 dB 1101 = 39 dB 1110 = 40 dB 1111 = Not defined	0…0

Table 21. DEC: Decoder Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
106h	LineOSel	[1:0]	Line select 00 = normal operation 01 = normal operation 10 = route Line input to Line output 11 = route Mic input to Line output	0…0
	SpkSel	[3:2]	Speaker select 00 = normal operation 01 = route Mic input to speaker output 10 = route Line input to speaker output 11 = Speaker output equals 0 (Vc on each side)	0…0
	LineOGn	[5:4]	Gain of Line Output 00 = Line output equals zero (Vc on each side) 01 = 4 dB gain 10 = -2 dB gain 11 = -8 dB gain	0…0
	SpkOGn	[7:6]	Gain of Speaker Output 00 = Speaker output equals zero (VC on each side) 01 = 4 dB gain 10 = -2 dB gain 11 = -8 dB gain	0…0
	LineOEn	[8]	Enable control of Line Output 0 = disable 1 = enable	0
	SpkOEn	[9]	Enable control of Speaker Output 0 = disable 1 = enable	0

Table 22. RXCTL: Rx Control Register

Addr.	Bit Name	Bit	Description	
107h	RxPga1GC	[2:0]	Gain Control for PGA1, in addition to nominal gain of Tune[13] 000 = 15 dB 001 = 16 dB 010 = 17 dB 011 = 18 dB 100 = 19 dB 101 = not defined 110 = not defined 111 = not defined	0…0
	RxPga2GC	[4:3]	Gain Control for PGA2, in addition to nominal gain of Tune[14] 00 = 12 dB gain 01 = 13 dB gain 10 = 14 dB gain 11 = 15 dB gain	0…0
	IFLpbk	[5]	Loopback of Tx modulator output to Rx PGA input 0 = normal mode 1 = loop back mode	0
	RxClbr	[6]	Control for Rx calibration (increase bandwidth of Rx low pass filter) 0 = normal mode 1 = calibration mode	0
	BypFIR	[8]	Bypass control of RxFIR 0 = Normal operation 1 = Bypass	0
	RxAna	[11:9]	Mux select for analog receive path 000 = RF (→ normal mode) 001 = Test (→ Rx Continuous Time Filter selects test input, which is also the Rx baseband input for cameleon mode) 010 = TX (→ Transmit Loopback: TxI to RxI & TxQ to RxQ) 011 = Reserved 100 = Gnd (→ Analog Ground, vc)	0…0

Table 23. TXCTL: Tx Control Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
108h	Reserved	[13:0]	Reserved	0…0
	TxInhbtDis	[15:14]	Control TxInhibit signal of watchdog 00 = Reserved 01 = disable tx_inhibit from ticloop-lock-detect-watchdog 10 = disable tx_inhibit from burststore-watchdog 11 = disable tx_inhibit completely	0…0

Table 24. GPO: General Purpose Output Registers, GPO0 to GPO11

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
10Eh - 119h	IFS	[0]	Enables general IFS to GPO	0
	TWBx	[1]	Enables Synthesizer bits to GPO Synclk to GPO0, GPO4, GPO8 Syndata to GPO1, GPO5, GPO9 Syn0rate to GPO2, GPO6 Syn1rate to GPO3, GPO7	0
	TxEn1	[2]	Enables TxEn1 (IFS[13]) to GPO	0
	TxEn2	[3]	Enables TxEn2 (IFS[12]) to GPO	0
	AntEn	[4]	Enables AntEn (IFS[10]) to GPO	0
	TxRx	[5]	Enables TxRx (IFS[8]) to GPO	0
	RxEn1	[6]	Enables RxEn1 (IFS[6]) to GPO	0
	RxEn2	[7]	Enables RxEn2 (IFS[5]) to GPO	0
	SynEn	[8]	Enables SynEn (IFS[4]) to GPO	0
	SynFast	[9]	Enables SynFast (IFS[1]) to GPO	0
	AUX	[10]	Enables general AUX to GPO	0
	AuxAnt	[11]	Enables AuxAnt (MASEN[1]) to GPO	0
	LoBand	[12]	Enables LoBand (TUNE[1]) to GPO	0
	HiBand	[13]	Enables HiBand (TUNE[0]) to GPO	0
	BAND	[14]	Enables general BAND to GPO	0
	INVGPO	[15]	Inverts GPO output	0
Note:	Address x10E - x119: GPO0 - GPO11 Each register for each GPOx has the same configuration.			

Table 25. MSCCTL: Miscellaneous Control Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
11Bh	SlowSlew	[1:0]	Slew rate control of slow output pads 00 = 3 ns @ 20 pF 01 = 5 ns @ 20 pF 10 = 9 ns @ 20 pF 11 = tristate	0…0
	FastSlew	[3:2]	Slew rate control of fast output pads 00 = 3 ns @ 20 pF 01 = 5 ns @ 20 pF 10 = 9 ns @ 20 pF 11 = tristate	0…0
	TSense	[4]	Control for Temperature Sensor 0 = disable 1 = enable	0

Table 26. ADC Control: Auxiliary ADC Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
120h	Reserved	[0]	Reserved	0
	Reserved	[1]	Reserved	0
	Reserved	[2]	Reserved	0
	ADCGn	[4:3]	Gain for ADC measurement 00 = 0 dB 01 = 12 dB 10 = 24 dB 11 = not defined	0…0
	ADCSel	[9:5]	MSD calibration selection for ADC measurement XX000 = AUXADC+, AUXADC- XX001 = Reserved XX010 = Reserved XX011 = Reserved XX100 = Reserved 00101 = MIC_BIAS selection: Temp sensor and Vc 01101 = Reserved 10101 = Reserved 11101 = MIC_BIAS selection: Temp sensor and Vc 00110 = Reserved 01110 = Reserved 10110 = Reserved 11110 = Reserved XX111 =Gnd	0…0
	MIC_BIAS	[10]	Control of MIC_BIAS 0 = disabled 1 = enabled	0
	CALAdcOff	[11]	Control offset to ADC output in calibration mode 0 = unsigned 1 = signed	0
	Reserved	[15:12]	Reserved	0…0

Table 27. CDCTST1: Codec Test Register 1

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
126h	BypDiv	[0]	Codec clock divider bypass. 0 = codec runs at 4MHz, divided down from 19.5 MHz (normal operation) 1 = divider is bypassed and codec runs at 19.5 MHz	0
	slowclkb	[1]	Codec analog clock control. 0 = codec analog is running at 1 MHz (normal operation) 1 = codec analog is running at 2 MHz	0
	enclk	[2]	Codec master clock enable. 0 = codec clocks are only enabled if needed 1 = codec clocks are forced on	0
	Clr_rxinteg	[3]	Encoder integrator clear. 0 = normal operation 1 = clear	0
	Clr_txinteg	[4]	Decoder integrator clear. 0 = normal operation 1 = clear	0
	ADCCtrl	[6:5]	00 = encoder path disabled 01 = LPF and HPF disable, SINC enabled 10 = HPF disabled, LPF and SINC enabled 11 = encoder fully powered	0…0
	LdAC2ADC	[7]	Digital loop back control. 0 = digital loop back disabled (normal operation) 1 = loop decoder DAC output into encoder SINC	0
	TxGn	[9:8]	Decoder path SINC gain selection. 00 = 0 dB 01 = +6 dB 10 = +12 dB 11 = -6 dB	0…0
	SelDACClk	[10]	Decoder DAC and analog clock selection. 0 = clock is 19.5 MHz / 16 (normal operation) 1 = clock is same as encoder clock, 1MHz	0
	TxICtrl	[11]	Decoder path filter control. 0 = normal operation 1 = bypass all filters and feed data directly into the DAC	0
	DACCtrl	[13:12]	00 = decoder powered down 01 = reserved 10 = IIR disabled, SINC enabled 11 = decoder fully functional	0…0
	Clr_cdc	[14]	Codec software reset. 0 = normal operation 1 = completely reset codec (same as applying POR)	0
	IFloop	[15]	Serial interface loop. 0 = normal operation 1 = serial interface loop (shift in, shift out)	0

Table 28. CDCTST2: Codec Test Register 2

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
127h	OSR	[5:0]	Codec oversampling ratio selection. 0: preselects oversampling ratio to 250 (default) 1 to 127: actual oversampling ratio is calculated according to following equation. actualOSR = (OSR+64)*2. The clocks follow the relationship: Interface strobe = codec clock / (2 * actualOSR) 8 kHz = 4 MHz / (2 * 250)	0…0
	TopMx	[9:8]	Top mux control. 00 = output encoder data to encdata pin (normal operation) 01 = output internal 16 kHz kick on encdata pin 10 = feed through output of CkGenMx 11 = feed through output of DACMx	0
	CkGenMx	[11:10]	Clock generator mux control. (to route its output to encdata, TopMx is set to 10) 00 = disable mux (output 0) 01 = observe clkcodec 10 = observe dacclk4 11 = observe clr_b	0…0
	CkMx	[13:11]	Codec clock mux control (to route its output to encdata, TopMx is set to 01) 00 = disable mux (output 0) 01 = observe txiclk 10 = observe dacclk 11 = observe adcclk	0…0
	DACMx	[15:14]	Multiplexer control (to route its output to encdata, TopMx is set to 11) 00 = disable mux (output 0) 01 = Bypass digital filters, (route ADC 1-bit output to encdata) 10 = Route DAC 1-bit output to encdata 11 = feed through output of CkMx	0…0

Table 29. CDCTST3: Codec Test Register 3

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
128h	TstADC	[0]	Test control of ADC 0 = normal mode 1 = test mode: ADC takes line_inp/line_inm as input	0
	TstSCF	[1]	Test control of Switch Capacitor Filter 0 = normal mode 1 = test mode: SCF output is connected to test_iop/test_iom	0
	TstSpk	[2]	Test control of Speaker 0 = normal mode 1 = test mode: Drive Speaker Driver from line_inp/line_inm	0
	TstLine	[3]	Test control of Line 0 = normal mode 1 = test mode: Drive Line Driver from line_inp/line_inm	0
	TstDig	[4]	Test control of digital blocks 0 = normal mode 1 = test mode: Feed digital decimation filter directly from line_inp	0
	ADCSel	[8]	Select control of ADC 0 = Normal operation 1 = Mute ADC	0
	SCFSel	[9]	Select control of Switch Capacitor Filter 0 = Normal input for SCF 1 = Loop back ADC 1 bit to SCF	0
	DitherSel	[12]	Select control of dither 0 = Dither on 1 = Dither off	0
	Mic_rxf_s	[13]	Select control of Mic mode 0 = Set Mic input to differential mode 1 = Set Mic input to single ended mode	0
	Line_rxf_s	[14]	Select control of Line mode 0 = Set Line input to differential mode 1 = Set Line input to single ended mode	0
	LpLnSpk	[15]	Control of line speaker 0 = Normal input for AAF 1 = Loop back Line or Speaker out	0

Table 30. CDCTST4: Codec Test Register 4

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
129h	PdbRefs	[0]	Power down control of references 0 = power down 1 = power up	0
	PdbADC	[1]	Power down control of ADC 0 = power down 1 = power up	0
	PdbAAF	[2]	Power down control of Anti Aliasing Filter 0 = power down 1 = power up	0
	PdbSCF	[3]	Power down control of Switch Capacitor Filter 0 = power down 1 = power up	0

Table 31. RXTST: Receive Test Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
12Ah	OffstEn	[0]	Control for offset canceling in Rx path 0 = disabled 1 = enabled	0
	TstRxDSM	[1]	Control test mode for Delta Sigma 0 = normal mode 1 = test mode	0
	TstPga3	[2]	Control test mode for PGA3 0 = normal mode 1 = test mode	0
	RxClkByp	[12]	Test mode control for digital Rx pattern test, which generates the symbol clock in the digital domain 0 = normal mode 1 = test mode	0
	RxShortEn	[13]	Control for shorting the two Rx inputs on the RF side 0 = normal mode (not shorted) 1 = test mode inputs shortest	0
	ISEL	[14]	Swap I and Q channels when doing Tx loopback 0 = normal mode 1 = swapped mode	0
	TstRxLp	[15]	Loopback of Codec Tx-path to regular Rx-FIR 0 = disabled 1 = enabled	0

Table 32. TXTST: Transmit Test Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
12Bh	TstTxCtf	[2:0]	Test selection for continuous time filter 000 = Rx: Normal mode / Tx: Normal mode 001 = Rx: Normal mode / Tx: CTF test mode 010 = Rx: loopback PGA output to Tx / Tx: Rx-Loop back 011 = Rx: loopback Rx low pass filter to Tx / Tx: Rx-Loop back 100 = Rx: loopback mixer output to Tx / Tx: Rx-Loop back 101 = not defined 110 = not defined 111 = not defined	0…0
	Reserved	[3:14]	Reserved	00h
	Aux	[15]	Test AuxADCoutput (Route MonADC to GPOs) 0 = normal mode 1 = test mode	0

Table 33. MSCTST: Miscellaneous Test Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
12Ch	BypSynth	[0]	Switch for Synth_en bypass 0 = disable 1 = enable	0
	ADC2GPO	[1]	Control bit, which routes AuxADC output to GPOs 0 = test mode disabled 1 = test mode enabled (AuxADC is routed to GPOs)	0
	Reserved	[2:15]	Reserved	00h

Table 34. RXPD: Receive Power Down Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
12Dh	RxDigPd	[0]	Powerdown Control of digital receive circuit 0 = power up 1 = power down	0
	RxAdcIPd	[1]	Powerdown Control of receive ADC I-path 0 = power up 1 = power down	0
	RxAdcQPd	[2]	Powerdown Control of receive ADC Q-path 0 = power up 1 = power down	0
	RxPga3IPd	[3]	Powerdown Control of receive PGA3 I-path 0 = power up 1 = power down	0
	RxPga3QPd	[4]	Powerdown Control of receive PGA3 Q-path 0 = power up 1 = power down	0
	RxLpfIPd	[5]	Powerdown Control of receive low pass filter I-path 0 = power up 1 = power down	0
	RxLpfQPd	[6]	Powerdown Control of receive low pass filter Q-path 0 = power up 1 = power down	0
	RxPga2IPd	[7]	Powerdown Control of receive PGA2 I-path 0 = power up 1 = power down	0
	RxPga2QPd	[8]	Powerdown Control of receive PGA3 Q-path 0 = power up 1 = power down	0
	RxMixPd	[10:9]	Powerdown Control of receive mixer path 0 = power up 1 = power down	0…0
	RxDivPd	[11]	Powerdown Control of receive divider 0 = power up 1 = power down	0
	RxCmfbPd	[12]	Powerdown Control of receive common mode feedback 0 = power up 1 = power down	0
	RxPga1Pd	[13]	Powerdown Control of PGA1 0 = power up 1 = power down	0
	RxBiasPd	[14]	Powerdown Control of Bias 0 = power up 1 = power down	0

Table 35. TXPD1: Transmit Power Down Register 1

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
12Eh	TxDigPd	[0]	Powerdown Control of digital transmit circuit 0 = power up 1 = power down	0
	PacDigPd	[1]	Powerdown Control of digital circuit of Power Amplifier 0 = power up 1 = power down	0
	TxDacIPd	[2]	Powerdown Control of transmit DAC I-path 0 = power up 1 = power down	0
	TxDacQPd	[3]	Powerdown Control of transmit DAC Q-path 0 = power up 1 = power down	0
	TxScfIPd	[4]	Powerdown Control of transmit switch capacitor filter I-path 0 = power up 1 = power down	0
	TxScfQPd	[5]	Powerdown Control of transmit switch capacitor filter Q-path 0 = power up 1 = power down	0
	TxCtfIPd	[6]	Powerdown Control of transmit continuous time filter I-path 0 = power up 1 = power down	0
	TxCtfQPd	[7]	Powerdown Control of transmit continuous time filter Q-path 1 = power down	0
	Reserved	[9:15]	Reserved	00h

Table 36. TXPD2: Transmit Power Down Register 2

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
12Fh	TxIQModPd	[0]	Powerdown Control of transmit IQ modulator 0 = power up 1 = power down	0
	TxBiasPd	[1]	Powerdown Control of transmit bias circuit 0 = power up 1 = power down	0
	TxDivPd	[2]	Powerdown Control of transmit divider circuit 0 = power up 1 = power down	0
	Reserved	[3:15]	Reserved	00h

Table 37. REGPD: Regulator Power Down Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
131h	VCODEC	[0]	Powerdown Control of analog Codec VDD 0 = power up 1 = power down	0
	VA1	[1]	Powerdown Control of analog VA1 0 = power up 1 = power down	0
	VAUX3	[2]	Powerdown Control of analog VAUX3 0 = power up 1 = power down	0
	VAUX1	[3]	Powerdown Control of analog VAUX1 0 = power up 1 = power down	0
	VAUX4	[4]	Powerdown Control of analog VAUX4 0 = power up 1 = power down	0
	Reserved	[5]	Set to zero at all times.	0
	VA2	[6]	Powerdown Control of analog VA2 0 = power up 1 = power down	0
	VAUX2	[7]	Powerdown Control of analog VAUX2 0 = power up 1 = power down	0
	VXTAL	[8]	Powerdown Control of analog VXTAL 0 = power up 1 = power down	0

Table 38. MASXO: Master XO Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
13Eh	SysReset	[0]	Trigger watchdog to reset system (if watchdog enabled)	0
	Reserved	[1]	Reserved	0
	Reserved	[2]	Reserved	0
	Reserved	[3]	Reserved	0
	XtlACtrl	[4]	Switch of amplitude control loop 0 = enabled 1 = disabled	0
	TstCap9	[5]	Control of test mode for fine cap array 0 = disabled 1 = enabled	0
	TstCap	[6]	Control for cap-array test block 0 = powered down 1 = powered up Enable test mode, which routes following signals to GPOs: cap_clk to GPO0, cap_1bit to GPO1 0 = normal mode 1 = test mode	0
	TstRange	[7]	Control for extended capacitor test range 0 = normal range 1 = extended range	0
	CapTestIO	[8]	Switch of test mode for coarse cap array 0 = enable output cap array 1 = enable input cap array	0
	Reserved	[9]	Reserved	0
	Reserved	[10]	Reserved	0
	Xtl_amp	[11]	Amplitude control 0 = peak equals to 1.00 V 1 = peak equals to 1.15 V	0

Table 39. MASEn: Master Enable Register

Addr.	Bit Name	Bit	Description (Default = 0000h)	Default Value
13Fh	MtxEn	[0]	Master Tx Enable	0
	AuxAnt	[1]	Select Auxiliary Antenna Port	0
	Reserved	[2]	Reserved	0
	Reserved	[3]	Reserved	0
	SynthEn	[4]	Enable Synthesizer	0
	WDEn	[5]	Enable Watch Dog	0
	CalEn	[6]	Enable Calibration ADC Function	0
	TxPwrEn	[7]	Enable Tx power control DAC (overrides auto-enable)	0
	MonRxEn	[8]	Monitor Burst Enable (Inhibit Rx functions except Rx serial I/O to BP during monitor slot if this bit is cleared	0
	AuxDacEn	[9]	Enable Auxiliary Control DAC’s	0
	NormRxEn	[10]	Receive Burst Enable (Inhibit Rx functions except Rx serial I/O to BP during receive slot if this bit is cleared)	0
	MicRef	[11]	Enable MIC bias of CODEC	0
	EncodEn	[12]	Enable Encoder Function (if Encoder-En and Decoder-En are both zero, the CODEC clocks stop)	0
	DecodEn	[13]	Enable Decoder Function (if Encoder-En and Decoder-En are both zero, the CODEC clocks stop)	0
	IFSEn	[15:14]	Enable Intra-Frame Sequencer 00 = Disable IFS and reset IFS output register and address 01 = Inhibit IFS operation 10 = N/A 11 = IFS fully operational	0

Table 40. GPOSt: GPO Status Register 1

Addr.	Bit Name	Bit	Description	Default Value
142h	GpoMon	[11:0]	Monitor Value of GPOs ***Note***: not strobed	
Note. *Status bits do not have default values.*				

Table 41. RXST1: Receive Status Register 1

Addr.	Bit Name	Bit	Description	Default Value
14Bh	Adc1Mon	[7:0]	1st strobed value of monitor ADC (calstrobe for CAL, Watchdog) ***Note***: strobed with clk_cal (540 kHz) and cal_strobe	
	Adc2Mon	[15:8]	2nd strobed value of monitor ADC (calstrobe for PAC, Watchdog) ***Note***: strobed with clk_cal (540 kHz) and cal_strobe	
Note: Status bits do not have default values.				

Table 42. RXST2: Receive Status Register 2

Addr.	Bit Name	Bit	Description	Default Value
14Dh	SatP	[0]	Positive saturation detected in CODEC	
	SatN	[1]	Negative saturation detected in CODEC	
Note. *Status bits do not have default values.*				

Table 43. VRF Output Voltage Tuning

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = FBh)</th><th>Default Value</th></tr>
<tr><td>01h</td><td>Reserved</td><td>[7]</td><td>Reserved</td><td>1</td></tr>
<tr><td></td><td>Overload</td><td>[6]</td><td>Overload protection
1 = Enabled
0 = Disabled</td><td>1</td></tr>
<tr><td></td><td>Reserved</td><td>[5:4]</td><td>Reserved</td><td>1</td></tr>
<tr><td></td><td>VRF Tune</td><td>[3:0]</td><td>VRF voltage tuning
<table>
<tr><th>Hex Value</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>VRF</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2.25V</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2.30V</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2.35V</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>2.40V</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>2.45V</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>2.50V</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>2.55V</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>2.60V</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>2.65V</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>2.70V</td></tr>
<tr><td>A</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2.75V</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2.80V</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2.85V</td></tr>
<tr><td>D</td><td>1</td><td>1</td><td>0</td><td>1</td><td>2.90V</td></tr>
<tr><td>E</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2.95V</td></tr>
<tr><td>F</td><td>1</td><td>1</td><td>1</td><td>1</td><td>3.00V</td></tr>
</table>
</td><td>1011</td></tr>
</table>

Table 44. Override Control Registers

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = 80h)</th><th>Default Value</th></tr>
<tr><td>02h</td><td>Reset value</td><td>[7:6]</td><td>Power down reset value selection
<table>
<tr><th>[7]</th><th>[6]</th><th>Power down Reset value</th></tr>
<tr><td>0</td><td>0</td><td>Disabled</td></tr>
<tr><td>0</td><td>1</td><td>-4%</td></tr>
<tr><td>1</td><td>0</td><td>-8%</td></tr>
<tr><td>1</td><td>1</td><td>-12%</td></tr>
</table></td><td>1000</td></tr>
<tr><td></td><td>VRF control</td><td>[5]</td><td>VRF control
0 = pin
1 = register value</td><td>0</td></tr>
<tr><td></td><td>VRF</td><td>[4]</td><td>VRF value
0 = off
1 = on</td><td>0</td></tr>
<tr><td></td><td>VTIC control</td><td>[3]</td><td>VTIC control
0 = pin
1 = register value</td><td>0</td></tr>
<tr><td></td><td>VTIC</td><td>[2]</td><td>VTIC value
0 = off
1 = on</td><td>0</td></tr>
<tr><td></td><td>VUHF control</td><td>[1]</td><td>VUHF control
0 = pin
1 = register value</td><td>0</td></tr>
<tr><td></td><td>VUHF</td><td>[0]</td><td>VUHF value
0 = off
1 = on</td><td>0</td></tr>
</table>

Table 45. Power Management Control Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = CEh)</th><th>Default Value</th></tr>
<tr><td>03Eh</td><td>Reserved</td><td>[7]</td><td>Reserved</td><td>1</td></tr>
<tr><td></td><td>SIM voltage</td><td>[6]</td><td>SIM voltage selection
0 = 1.8 V
1 = 2.8 V</td><td>1</td></tr>
<tr><td></td><td>Reserved</td><td>[5]</td><td>Reserved</td><td>0</td></tr>
<tr><td></td><td>VCORE voltage</td><td>[4:1]</td><td>VCORE voltage selection
<table>
<tr><th>HEX Value</th><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>%</th><th>VCORE @1.2V</th><th>VCORE @1.7V</th><th>VCORE @2.4V</th><th>VCORE @2.8V</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>-6.3%</td><td>1.1249</td><td>1.5929</td><td>2.2488</td><td>2.6236</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>-5.4%</td><td>1.1357</td><td>1.6082</td><td>2.2704</td><td>2.6488</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>-4.5%</td><td>1.1464</td><td>1.6235</td><td>2.2920</td><td>2.6740</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>-3.6%</td><td>1.1571</td><td>1.6388</td><td>2.3136</td><td>2.6992</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>-2.7%</td><td>1.1679</td><td>1.6541</td><td>2.3352</td><td>2.7244</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>-1.8%</td><td>1.1786</td><td>1.6694</td><td>2.3568</td><td>2.7496</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>-0.9%</td><td>1.1893</td><td>1.6847</td><td>2.3784</td><td>2.7748</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1.2000</td><td>1.7000</td><td>2.4000</td><td>2.8000</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>+0.9%</td><td>1.2101</td><td>1.7153</td><td>2.4216</td><td>2.8252</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>+1.8%</td><td>1.2214</td><td>1.7306</td><td>2.4432</td><td>2.8504</td></tr>
<tr><td>A</td><td>1</td><td>0</td><td>1</td><td>0</td><td>+2.7%</td><td>1.2321</td><td>1.7459</td><td>2.4648</td><td>2.8756</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>1</td><td>1</td><td>+3.6%</td><td>1.2428</td><td>1.7612</td><td>2.4864</td><td>2.9008</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>0</td><td>0</td><td>+4.5%</td><td>1.2535</td><td>1.7765</td><td>2.5080</td><td>2.9260</td></tr>
<tr><td>D</td><td>1</td><td>1</td><td>0</td><td>1</td><td>+5.4%</td><td>1.2648</td><td>1.7918</td><td>2.5296</td><td>2.9512</td></tr>
<tr><td>E</td><td>1</td><td>1</td><td>1</td><td>0</td><td>+6.3%</td><td>1.2749</td><td>1.8071</td><td>2.5512</td><td>2.9764</td></tr>
<tr><td>F</td><td>1</td><td>1</td><td>1</td><td>1</td><td>+7.2%</td><td>1.2857</td><td>1.8224</td><td>2.5728</td><td>3.0016</td></tr>
</table></td><td>0111</td></tr>
</table>

	Phone	[0]	Phone on/off 0 = off 1 = on (Required to keep the system on.)	0

Table 46. Low-Drop-Out VRF Control Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = 01h)</th><th>Default Value</th></tr>
<tr><td rowspan="2">04h</td><td>Polarity control</td><td>[7:5]</td><td>Polarity control
<table>
<tr><th>[7]</th><th>[6]</th><th>[5]</th><th colspan="3">A/B/C Values</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>EN_1</td><td>EN_2</td><td>EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>EN_1</td><td>EN_2</td><td>/EN_3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>EN_1</td><td>/EN_2</td><td>EN_3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>EN_1</td><td>/EN_2</td><td>/EN_3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>/EN_1</td><td>EN_2</td><td>EN_3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>/EN_1</td><td>EN_2</td><td>/EN_3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>/EN_1</td><td>/EN_2</td><td>EN_3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>/EN_1</td><td>/EN_2</td><td>/EN_3</td></tr>
<tr><td colspan="6">/Bold indicates inverted polarity</td></tr>
</table></td><td>000</td></tr>
<tr><td>RTCS_CS</td><td>[4:0]</td><td>Real time control combination selection (EN_1, EN_2, EN_3)
<table>
<tr><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN_1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>EN_2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>EN_3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>EN_1 x EN_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>EN_1 x EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>EN_2 x EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>EN_1+ EN_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>EN_1+ EN_3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>EN_2+ EN_3</td></tr>
</table></td><td>00001</td></tr>
</table>

Table 47. Low-Drop-Out VTIC Control Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = 02h)</th><th>Default Value</th></tr>
<tr><td rowspan="2">05h</td><td>Polarity control</td><td>[7:5]</td><td>Polarity control
<table>
<tr><th>[7]</th><th>[6]</th><th>[5]</th><th colspan="3">A/B/C Values</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>EN_1</td><td>EN_2</td><td>EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>EN_1</td><td>EN_2</td><td>/EN_3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>EN_1</td><td>/EN_2</td><td>EN_3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>EN_1</td><td>/EN_2</td><td>/EN_3</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>/EN_1</td><td>EN_2</td><td>EN_3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>/EN_1</td><td>EN_2</td><td>/EN_3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>/EN_1</td><td>/EN_2</td><td>EN_3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>/EN_1</td><td>/EN_2</td><td>/EN_3</td></tr>
<tr><td colspan="6">/Bold indicates inverted polarity</td></tr>
</table></td><td>0</td></tr>
<tr><td>RTCS_CS</td><td>[4:0]</td><td>Real time control combination selection (EN_1, EN_2, EN_3)
<table>
<tr><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN_1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>EN_2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>EN_3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>EN_1 x EN_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>EN_1 x EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>EN_2 x EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>EN_1+ EN_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>EN_1+ EN_3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>EN_2+ EN_3</td></tr>
</table></td><td>0001</td></tr>
</table>

Table 48. Low-Drop-Out VUHF Control Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = 01h)</th><th>Default Value</th></tr>
<tr><td rowspan="2">06h</td><td>Polarity control</td><td>[7:5]</td><td>Polarity control
<table>
<tr><th>[7]</th><th>[6]</th><th>[5]</th><th colspan="3">A/B/C Values</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>EN_1</td><td>EN_2</td><td>EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>EN_1</td><td>EN_2</td><td>**/EN_3**</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>EN_1</td><td>**/EN_2**</td><td>EN_3</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>EN_1</td><td>**/EN_2**</td><td>**/EN_3**</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>**/EN_1**</td><td>EN_2</td><td>EN_3</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>**/EN_1**</td><td>EN_2</td><td>**/EN_3**</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>**/EN_1**</td><td>**/EN_2**</td><td>EN_3</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>**/EN_1**</td><td>**/EN_2**</td><td>**/EN_3**</td></tr>
<tr><td colspan="6">**/Bold indicates inverted polarity**</td></tr>
</table>
</td><td>0</td></tr>
<tr><td>RTCS_CS</td><td>[4:0]</td><td>Real time control combination selection (**EN_1**, **EN_2**, **EN_3**)
<table>
<tr><th>[4]</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>Result</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>EN_1</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>EN_2</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>EN_3</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>EN_1 x EN_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>EN_1 x EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>EN_2 x EN_3</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>EN_1+ EN_2</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>EN_1+ EN_3</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>EN_2+ EN_3</td></tr>
</table>
</td><td>0001</td></tr>
</table>

Table 49. Power-up Status Register

Addr.	Bit Name	Bit	Description	Default Value
08h	Reserved	[7:4]	Reserved	
	PWR_KEY_H	[3]	Power up source = PWR_KEY_H 0 = not asserted 1 = asserted	
	DTR	[2]	Power up source = DTR 0 = not asserted 1 = asserted	
	ALARM	[1]	Power up source = ALARM 0 = not asserted 1 = asserted	
	PWR_KEY_L	[0]	Power up source = PWR_KEY_L 0 = not asserted 1 = asserted	
Note: Status bits do not have default values.				

Table 50. VTIC Voltage Tuning and Control

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = FBh)</th><th>Default Value</th></tr>
<tr><td>09h</td><td>Reserved</td><td>[7]</td><td>Reserved</td><td>1</td></tr>
<tr><td></td><td>Overload</td><td>[6]</td><td>Overload protection
1 = Enabled
0 = Disabled</td><td>1</td></tr>
<tr><td></td><td>Reserved</td><td>[5:4]</td><td>Reserved</td><td>11</td></tr>
<tr><td></td><td>VTIC Tune</td><td>[3:0]</td><td>VTIC voltage tuning
<table>
<tr><th>Hex Value</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>VRF</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2.25V</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2.30V</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2.35V</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>2.40V</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>2.45V</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>2.50V</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>2.55V</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>2.60V</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>2.65V</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>2.70V</td></tr>
<tr><td>A</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2.75V</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2.80V</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2.85V</td></tr>
<tr><td>D</td><td>1</td><td>1</td><td>0</td><td>1</td><td>2.90V</td></tr>
<tr><td>E</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2.95V</td></tr>
<tr><td>F</td><td>1</td><td>1</td><td>1</td><td>1</td><td>3.00V</td></tr>
</table>
</td><td>1011</td></tr>
</table>

Table 51. Bandgap Voltage Tuning Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = 07h)</th><th>Default Value</th></tr>
<tr><td>0Ah</td><td>Reserved</td><td>[7:4]</td><td>Reserved</td><td>0</td></tr>
<tr><td></td><td>Bandgap tune</td><td>[3:0]</td><td>Bandgap output voltage tuning
<table>
<tr><th>HEX Value</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>Bandgap Voltage</th><th>VIO Voltage</th><th>Variation in %</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1.0976</td><td>2.562</td><td>-8.5</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1.1111</td><td>2.593</td><td>-7.4</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1.1251</td><td>2.624</td><td>-6.3</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1.1393</td><td>2.657</td><td>-5.1</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1.1539</td><td>2.694</td><td>-3.8</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1.1689</td><td>2.724</td><td>-2.6</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1.1842</td><td>2.764</td><td>-1.3</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1.2000</td><td>2.800</td><td>0</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1.2162</td><td>2.836</td><td>1.3</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1.2328</td><td>2.876</td><td>2.7</td></tr>
<tr><td>A</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1.2499</td><td>2.918</td><td>4.2</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1.2675</td><td>2.957</td><td>5.6</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1.2856</td><td>2.999</td><td>7.1</td></tr>
<tr><td>D</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1.3042</td><td>3.044</td><td>8.7</td></tr>
<tr><td>E</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1.3234</td><td>3.088</td><td>10.3</td></tr>
<tr><td>F</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1.3431</td><td>3.133</td><td>11.9</td></tr>
</table>
</td><td>0111</td></tr>
</table>

Table 52. VUHF Voltage Tuning and Control

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = FBh)</th><th>Default Value</th></tr>
<tr><td>0Bh</td><td>Reserved</td><td>[7]</td><td>Reserved</td><td>1</td></tr>
<tr><td></td><td>Overload</td><td>[6]</td><td>Overload protection
1 = Enabled
0 = Disabled</td><td>1</td></tr>
<tr><td></td><td>Reserved</td><td>[5:4]</td><td>Reserved</td><td>11</td></tr>
<tr><td></td><td>VUHF Tune</td><td>[3:0]</td><td>VUHF voltage tuning
<table>
<tr><th>Hex Value</th><th>[3]</th><th>[2]</th><th>[1]</th><th>[0]</th><th>VRF</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>2.25 V</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>2.30 V</td></tr>
<tr><td>2</td><td>0</td><td>0</td><td>1</td><td>0</td><td>2.35 V</td></tr>
<tr><td>3</td><td>0</td><td>0</td><td>1</td><td>1</td><td>2.40 V</td></tr>
<tr><td>4</td><td>0</td><td>1</td><td>0</td><td>0</td><td>2.45 V</td></tr>
<tr><td>5</td><td>0</td><td>1</td><td>0</td><td>1</td><td>2.50 V</td></tr>
<tr><td>6</td><td>0</td><td>1</td><td>1</td><td>0</td><td>2.55 V</td></tr>
<tr><td>7</td><td>0</td><td>1</td><td>1</td><td>1</td><td>2.60 V</td></tr>
<tr><td>8</td><td>1</td><td>0</td><td>0</td><td>0</td><td>2.65 V</td></tr>
<tr><td>9</td><td>1</td><td>0</td><td>0</td><td>1</td><td>2.70 V</td></tr>
<tr><td>A</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2.75 V</td></tr>
<tr><td>B</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2.80 V</td></tr>
<tr><td>C</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2.85 V</td></tr>
<tr><td>D</td><td>1</td><td>1</td><td>0</td><td>1</td><td>2.90 V</td></tr>
<tr><td>E</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2.95 V</td></tr>
<tr><td>F</td><td>1</td><td>1</td><td>1</td><td>1</td><td>3.00 V</td></tr>
</table></td><td>1011</td></tr>
</table>

Table 53. MUX Control Register

<table>
<tr><th>Addr.</th><th>Bit Name</th><th>Bit</th><th>Description (Default = 02h)</th><th>Default Value</th></tr>
<tr><td>0Ch</td><td>Reserved</td><td>[7:6]</td><td>Reserved</td><td>0</td></tr>
<tr><td></td><td>CurrAmp GAIN</td><td>[5]</td><td>Current sense amplifier gain
0 - 20V / V, 1 - 10V / V,</td><td>0</td></tr>
<tr><td></td><td>Reserved</td><td>[4:3]</td><td>Reserved</td><td>0</td></tr>
<tr><td></td><td>Mux control</td><td>[2:0]</td><td>Selects which analog voltage is present on MUX_OUT pin
<table>
<tr><th>[2]</th><th>[1]</th><th>[0]</th><th>Selected</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>All OFF</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Current Sense</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>BAT_PK_IN</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DAC Voltage</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>VCHARGE</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>VBATTERY</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>VCORE</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>VIO</td></tr>
</table></td><td>010</td></tr>
</table>

Table 54. VGATE DAC Value Register

Addr.	Bit Name	Bit	Description (Default = 00h)	Default Value
0Dh	VGATE DAC value	[7:0]	By writing a DAC value register, enables the user to change voltage on VGATE pin to control eternal mosfet for charging the battery.	00h

Device Performance and Electrical and Mechanical Specifications

Table 55 lists the tables and figures that show the CX20524 performance, electrical, and mechanical specifications.

Table 55. Performance, Electrical, and Mechanical Specifications

Figure/Table	Title
Table 56	Transmit I/Q Performance Characteristics
Table 57	Transmit IF Performance Characteristics
Table 58	Receiver Performance Characteristics
Table 59	Receive Gain Settings (Input/Output)
Table 60	Receiver Frequency Selectivity
Table 61	MIC_IN/LINE_IN Performance Characteristics
Table 62	SPK_OUT/LINE_OUT Performance Characteristics
Table 63	Voltage, Current, and Temperature Maximum Ratings
Table 64	Voltage and Temperature Recommended Operating Limits
Table 65	Analog Signals Electrical Characteristics
Table 66	8-Bit Internal DAC for Charger Control
Table 67	Current Sense Amplifier
Table 68	Internally Pulled-Up Signals Electrical Characteristics
Table 69	Digital Signals Electrical Characteristics
Table 70	SIM Interface Electrical Specifications
Table 71	19.5 MHz Crystal Specifications
Table 72	System Voltage Regulator Electrical Specifications
Table 73	Reference Voltages
Table 74	Sleep Mode Active Functions
Figure 25	160-Pin FPBGA Package Dimensions

ESD Sensitivity

Caution The CX20524 is an Electrostatic Discharge (ESD) static-sensitive electronic device. The human body and test equipment can build electrostatic charges that can discharge without detection.

Do not operate or store CX20524 devices near strong electrostatic fields. Permanent damage may occur. Take proper ESD precautions.

Table 56. Transmit I/Q Performance Characteristics

Description	Performance	Units
At Tx I and Q Outputs		
Output Amplitude (driving high impedance or open circuit)	1 ± 0.05	Vpp diff
Output capacitive Load driving capability	20	pF diff
	45	
Output Resistive Load driving capability	20	kΩ diff
Output common mode	1.35 ± 0.05	V
Power supply rejection ratio	> 40	dB
Frequency for given PSRR	DC to > 1	MHz
Frequency for unity PSRR	> 10	MHz
Output impedance	2 ± 20 %	kΩ diff
Output impedance imbalance	< 3	%
DC offset - Unadjusted	± 10	mV
Adjustment range	> ± 80	mV
Step size	< 1	mV
Gain Balance - Unadjusted	< 1	%
Adjustment range	> ± 10	%
Step size	< 0.5	%
Quadrature error - Unadjusted	0.5	°
Adjustment range *	> ± 5	%
Step size	< 0.5	%
Total Harmonic Distortion	-60	dBc
Isolation between I and Q	> 60	dB
I vs Q frequency response match	Within 0 to 400	kHz
Relative Gain error (Gerr)	< 0.5	%
Ga·Gr /Gb	0.5 to 2.0	
Weighted Phase error (Perr)	0.25	°
Output Spectrum		
Frequency Range Bandwidth		
15 kHz 30 kHz	0	dB
100 kHz 30 kHz	-6 to -12	dB
200 kHz 30 kHz	< -36	dB
250 kHz 30 kHz	< -40	dB
400 kHz 30 kHz	< -70	dB
600 kHz to 1.8 MHz 30 kHz	< -80	dB
1.8 MHz to 3.0 MHz 100 kHz	< -90	dB
3.0 MHz to 6.0 MHz 100 kHz	< -78	dB
Above 6.0 MHz 100 kHz	< -90	dB
Maximum Output Noise		
Frequency Range Bandwidth		
0 to 200 kHz 30 kHz	-53	dBv
200 to 400 kHz 30 kHz	-53 to -71	dBv
400 to 600 kHz 30 kHz	-71 to -81	dBv
600 to 1800 kHz 30 kHz	-81 to -82	dBv
Above 1800 kHz 100 kHz	-82	dBv

Phase error in a Tx burst - peak	1	°
- RMS	0.5	°

Table 57. Transmit IF Performance Characteristics

Description	Performance	Units
At Tx IF output		
IF frequency	400	MHz
Output Amplitude (driving high impedance or open circuit)		dBVp diff
Output capacitive Load driving capability	45	pF diff
Output Resistive Load driving capability	20	KΩ diff
Output impedance		Ω diff
		fF
Output impedance imbalance	< 3	%
Carrier Feedthrough		
Unadjusted	<-37	dBc
Adjusted	< 50	dBc
Negative sideband suppression		
Unadjusted	> 28	dB
Adjusted	> 46	dB
Harmonic Distortion with ± 67 kHz tone from modulator	<-60 @ 2x	DBc
	<-55 @ 3x	dBc
	<-70 @ higher	dBc
Total signal around 3x carrier		
Without Tx IF filter	< -10	dBc
After Tx IF filter	< -60	dBc
Output Spectrum		
Frequency offset Bandwidth		
0 kHz 30 kHz	0	dB
100 kHz 30 kHz	-6 to -12	dB
200 kHz 30 kHz	< -36	dB
250 kHz 30 kHz	< -40	dB
400 kHz 30 kHz	< -70	dB
600 kHz to 1.8 MHz 30 kHz	< -80	dB
1.8 MHz to 3.0 MHz 100 kHz	< -90	dB
3.0 MHz to 6.0 MHz 100 kHz	< -78	dB
Above 6.0 MHz 100 kHz	< -90	dB
Maximum Output Noise		
Frequency Offset Bandwidth		
0 to 200 kHz 30 kHz	-53	dBv
200 to 400 kHz 30 kHz	-53 to -71	dBv
400 to 600 kHz 30 kHz	-71 to -81	dBv
600 to 1800 kHz 30 kHz	-81 to -82	dBv
Above 1800 kHz 100 kHz	-82	dBv
Phase error in a Tx burst - peak	3	°
- RMS	1.0	°

Table 58. Receiver Performance Characteristics

Parameter	Performance	Unit
Input Impedance		
Resistive	10	KΩ
Capacitive	<1	pF
Input Common Mode Range	1.35	V
Common Mode Rejection Ratio (for freq up to 1 GHz)	>40	dB
Power Supply Rejection Ratio at Baseband	>40	dB
Min Input Signal (Max gain)	-61	dBV
Max Input Signal (Max gain)	-30	dBV
Max Blocker @3 MHz (Max gain)	-27	dBV
Max Input Testing Baseband Signal	-2	dBV
Voltage Gain Range:		
Max Gain	24 ± 0.7	dB
Min Gain	0 ± 0.7	dB
Stage Gain Accuracy:		
LPF	± 0.2	dB
PGA3	± 0.5	dB
Gain Steps:		
LPF	12,6 ± 0.2	dB
PGA3	12,6 ± 0.25	dB
Input Referred Noise (Max gain)	-98.4	dBV
Input P1db:		
High Gain mode (Max gain)	-28	dBV
Low Gain mode (Max gain)	-5	
Power Consumption:		
High Gain mode (Max gain)	7.5	mA
Low Gain mode (Max gain)	6.5	

Table 59. Receive Gain Settings

Input Signal (dBV)		Total Gain	Gain Distribution (dB)				Output Signal (dBfs)		Maximum Input Referred Noise (dBV)	Minimum Input (dBV)
Min	Max		PGA1	MX	LPF	PGA3	Min	Max		
-88	-76	51 dB	15	12	12	12	-53.6	-23.6	-109	-55
-76	-70	45 dB	15	12	6	12	-29.6	-23.6		
-70	-64	39 dB	15	12	6	6	-29.6	-23.6		
-64	-54	33 dB	15	12	0	6	-29.6	-19.6		
-58	-52	27 dB	-9	12	12	12	-29.6	-23.6	-86	-31
-52	-46	21 dB	-9	12	6	12	-29.6	-23.6		
-46	-40	15 dB	-9	12	6	6	-29.6	-23.6		
-40	-34	9 dB	-9	12	0	6	-29.6	-23.6		
-34	-28	3 dB	-9	0	6	6	-29.6	-23.6		
-28	-22	-3 dB	-9	0	0	6	-29.6	-23.6	-62	-6

Table 60. Receiver Frequency Selectivity

Deviation from IF Center Frequency (kHz)	Attenuation (dB)	
	Min	Max
0-60	0	0.1
75	0	0.5
88	0.5	1.7
94	1.5	2.1
100	3.4	3.7
110	5	8
120	9	13
140	18	24
200	37	
Above 300	50	
Above 400	54	

Table 61. MIC_IN/LINE_IN Performance Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Gain Accuracy		-0.1	0	+0.1	dB
LPF -3 dB freq (0 dB gain)					kHz
Inband Ripple				0.1	dB
Group Delay				360	μsec
Input impedance (single ended)	Zin	38			kΩ
Input impedance variation		-20	0	20	%
Suppression @ 1 MHz		40			dB
Total Harmonic Distortion	THD			-55	dB
Mic In-Band Output Referred Noise					
-4 dB Mic gain setting				-84	dBVrms
0 dB Mic gain setting				-84	dBVrms
6 dB Mic gain setting				-84	dBVrms
12 dB Mic gain setting				-84	dBVrms
18 dB Mic gain setting				-84	dBVrms
24 dB Mic gain setting				-84	dBVrms
28 dB Mic gain setting				-80	dBVrms
Band=300-3.4 kHz					

Table 62. SPK_OUT/LINE_OUT Performance Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Gain Accuracy		-0.1	0	+0.1	dB
LPF -3dB freq (1.1 dB gain)			40		kHz
In-band Ripple				0.1	dB
Group Delay				360	μsec
Suppression @ 1 MHz			24		dB
Total Harmonic Distortion 2KOhmD	THD			-40	dB
Output Referred Noise				-98	dBVrms
Isolation Tx-Rx		70			dB
band=300Hz-3.4 kHz					

Table 63. Voltage, Current, and Temperature Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply voltage	VPOWER	- 0.5 to + 6.0	V
Input voltage	V_{IN}	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
Analog Inputs	V_{IN}	(V_{SS} - 0.3) to (V_{DD} + 0.3)	V
DC input clamp current	I_{IK}	± 10	mA
DC output clamp current	I_{OK}	± 50	mA
Static discharge voltage (25^0 C)	V_{ESD}	Human body model = ± 2500 Charged device model = ± 200	V
Latch up current (25^0 C)	I_{TRIG}	± 150	mA
Storage temperature range	I_{STG}	- 55 to +150	^{0}C
Note: All voltages referenced to ground (V_{SS})			

Table 64. Voltage and Temperature Recommended Operating Limits

Parameter	Symbol	Limits	Units
Supply voltage	VPOWER	+ 3.0 to + 5.6	V
Supply voltage	VCHARGE	4.5 to + 5.9	V
Operating ambient temperature range	T_A	- 40 to + 85	^{0}C

Table 65. Analog Signals Electrical Characteristics (1 of 2)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
Analog Input						
Receive Inputs (RXI, RXQ)						
Differential Input Signal Level				0.150	2	Vp-p
Differential Input Resistance			10			kΩ
Differential Input Capacitance					1	pF
Microphone and Line Input (MIC_IN+/MIC_IN-, LINE_I+/LINE_I-)		PGA gain = - 4 dB		3.2		VPP
Differential Input Signal Level		PGA gain = 0 dB		2		VPP
		PGA gain = 6 dB		1		VPP
		PGA gain = 12 dB		0.5		VPP
		PGA gain = 18 dB		0.25		VPP
		PGA gain = 24 dB		0.125		VPP
		PGA gain = 28 dB		0.0625		VPP
Input Impedance		PGA gain = - 4 dB		950		kΩ
		PGA gain = 24 dB		38		kΩ
Current Bias Resistor (RBIAS)		Resistor connected to ground	29.7	30	30.3	kΩ
Auxiliary ADC Input (AUXADC+/AUXADC-)						
Differential Input Signal Level					2	Vp-p
Input Common Mode Voltage				1.35		V
Differential Input Capacitance					3.2	pF
BAT_PK_IN						
Input voltage range	Vin		-0.3	-	5.0	V
Input resistance to ground	Rin		13.4	16.7	20.1	K•
Input capacitance	Cin		-	-	15	pF
VCHARGE						
Input voltage range	Vin		-0.3	-	5.5	V
Input impedance	Zin		190	240	290	k•
Input capacitance	Cin		-	-	15	pF
V_{Charge} – VBATTERY Comparator hysterosis	•V			± 10		mV
Analog Output						
Transmit I/Q Outputs (TX_I+ / TX_I- and TX_Q+ / TX_Q-)						
Output Signal Level		No load connected	0.95	1.0	1.05	V
Common Mode Voltage			1.34	1.35	1.36	V
Differential Load Resistance			20			kΩ
Differential Load Capacitance					20	pF
Output Impedance			1.6	2	2.4	kΩ
Transmit Power Control (PAC_OUT)						
Output Signal Level			0.3		2.4	V
Sourcing current					300	µA
Sinking current			300			µA
Output					0.25	kΩ
Speaker and Line Output (SPK+/SPK-, LINE_O+/LINE_O-)						
Differential Output Signal Level					3.8	Vp-p
Differential Load			32			Ω
Microphone Bias Voltage (MIC_BIAS)						
Bias Voltage				2.2		V
Source Current					1	mA
Analog Midrail Voltage Reference (VREF)	VC	0.1 µF cap. To ground required		1.35 ± 0.01		V
Negative Reference Voltage	VC_REF-	0.1 µF cap. To ground required		0.85 ± 0.01		V
Positive Reference Voltage	VC_REF+	0.1 µF cap. To ground required		1.85 ± 0.01		V

Codec Reference Voltage	VC_CODEC	0.1 µF cap. To ground required		1.35 ± 0.01		V

Table 65. Analog Signals Electrical Characteristics (2 of 2)

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
MUX_OUT						
Output voltage range	Vout	At Iout max	-0.3	-	2.5	V
Output impedance	Zout	At Iout max	-	-	1000	•
Output drive strength	Iout		100	-	200	•A
MUX Active Current	Ivdd		-	-	100	•A
MUX Sleep Current	Isleep		-	-	1	•A
VBATTERY Voltage gain	Gain1		0.2375	0.25	0.2625	V/V
VCHARGE Voltage gain	Gain2		0.2375	0.25	0.2625	V/V
VCORE Voltage gain	Gain3		0.2375	0.25	0.2625	V/V
VIO Voltage gain	Gain4		0.2375	0.25	0.2625	V/V
BAT_PK_IN	-		-	1	-	V/V
Current Sense Amplifier	-		-	1	-	V/V
DAC Voltage	-		-	1	-	V/V
VGATE						
Output voltage range	Vout	At Iout max	-0.3	-	5.0	V
Output impedance	Zout	At Iout max	-	-	100	•
Output drive strength	Iout		1	-	-	mA

Note: All voltages referenced to ground (Vss). Currents are positive flowing into the device.

Table 66. 8-Bit Internal DAC for Charger Control

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
Resolution	Vin		-	8	-	bit
Minimum output voltage on MUX_OUT	Voutmin	Register value = 00h	0	-	0.2	V
Maximum output voltage on MUX_OUT	Voutmax	Register value = FFh	2.35	2.4	2.45	V
Output voltage after reset	Voutreset	Register Value = 00h	-	0	0.2	V
Offset error	Voffset		-50	-	+50	mV
Full scale settling time	Tfull		-	100	-	•s
One LSB settling time	TLSB		-	10	-	•s
Active Current	Ivdd		-	-	100	•A
Sleep Current	Isleep		-	-	1	•A

Table 67. Current Sense Amplifier

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
Input voltage range	Vin		2.5	-	5.5	V
Input impedance	Zin		1e6	-	-	•
Input capacitance	Cin		-	-	15	pF
Input common-Mode range	Icm		5	-	-	V
Input offset voltage	Voffset		12	-	40	mV
Current to Voltage ratio, excluding the sense resistor variations, over the temperature and voltage ranges.	Gain	100 mA across 150 m• results in 1.50 V out on MUX_OUT AD5=1	9.5	10	10.5	V/V
Current to Voltage ratio, excluding the sense resistor variations, over the temperature and voltage ranges.	Gain	500 mA across 150 m• will result in 1.5 V out on MUX_OUT AD5=0	18	20	22	V/V
Amplifier Active Current	Ivdd		-	-	100	•A
Amplifier Sleep Current	Isleep		-	-	1	•A
Internal Sense Resistor	R_{Sense}		0.09	0.10	0.11	•
Max Current Capability of R_{Sense}	Imax (R_{Sense})			0.600	0.800*	A

***Note**: If charging currents are greater than 800 mA, connect an external 0.10 • resistor between ISN and ISP pins in parallel with* R_{Sense}.

Table 68. Internally Pulled-Up Signals Electrical Characteristics

Name	Direction	Supply	Strength		Minimum	Typical	Maximum	Units
PWR_KEY_L	Input	VPOWER	100 µA	Pulled up				
				Vil	-0.3	-	0.5	V
DTR	Input	VPOWER	100 µA	Pulled up				
				Vil	-0.3	-	0.5	V
VSEL0 and VSEL1	Input		1 µA	Pulled up				
				Vil	-0.3	-	0.5	V
ALARM	Input	VRTC	1 µA	Pulled up				
				Vil	-0.3	-	0.5	V

Table 69. Digital Signals Electrical Characteristics

Symbol	Parameters	Conditions	Minimum	Typical	Maximum	Units
MSD_RESET, SERIAL_CLOCK, SERIAL_DATA, EN_1, EN_2, EN_3, MSD_SLEEP, SIM_EN						
Vih	High level input voltage on pin.	I=1 µA (max)	1.5	-	VPOWER+0.3	V
Vil	Low level input voltage on pin.	I=-1 µA (max)	-0.3	-	0.5	V
Tr and Tf		Cin = Cout = 30 pF			100	ns
POR_OUT, FLASH_RESET, CHARGER_INT, PWR_KEY_OUT						
Voh	High level output voltage on pin.	I=750 µA (max)	VIO-0.4V	-	VIO+0.3	V
Vol	Low level output voltage on pin.	I=-750 µA (max)	-0.3	-	0.4	V
Tr and Tf		Cin = Cout = 30 pF			100	ns
ALARM						
Vih	High level input voltage on pin.	I=20 µA (max)	0.9	-	VRTC+0.3	V
Vil	Low level input voltage on pin.	I=-1 µA (max)	-0.3	-	0.5	V
PWR_KEY_H						
Vih	High level input voltage on pin.	I=20 µA (max)	1.5	-	VPOWER +0.3	V
Vil	Low level input voltage on pin.	I=-1 µA (max)	-0.3	-	0.5	V
All Other Digital Signals						
V_{IH}	Input high voltage	V_{DD} = 3.0 V	0.8 × V_{DD}			V
V_{IL}	Input low voltage	V_{DD} = 3.0 V			0.4	V
V_{OH}	Output high voltage	V_{DD} = 3.0 V, sourcing 100 µA	0.8 × V_{DD}			V
V_{OH}	Output low voltage	V_{DD} = 3.0 V, sinking 1.6 mA			0.4	V
C_{IN}	Input capacitance (inputs)	V_{DD} = 3.0 V			5	pF
C_L	Capacitive load (outputs)	V_{DD} = 3.0 V			20	pF
System Clock						
 V_{OH} V_{OL}	3.9 MHz Clock output Output High voltage Output Low voltage	 I_{OH} = 100 µA I_{OL} = 1.6 mA	 2.4		 0.4	 V V
GPO						
V_{OH} V_{OL}	Output High voltage Output Low voltage	I=-1 µA (max) I=-1 µA (max)	2.7 -0.3		2.88 0.4	V V
Tr and Tf		Cout = 20 pF			10	ns

Table 70. SIM Interface Electrical Specifications (1 of 2)

Symbol	Parameters	Conditions	Minimum	Typical	Maximum	Units
SIM CARD Side						
SIM VCC at 1.8 V						
Vcc		Icc=4 mA (max)	1.71	-	1.89	V
SIM VCC at 2.85 V						
Vcc		Icc=6 mA (max)	2.75	-	3.3	V
SIM_DATA_CARD at 1.8 V						
Voh	High level output voltage on pin.	Ioh=+20 µA (max)	1.32	-	1.89	V
Vol	Low level output voltage on pin.	Iol=-200 µA (max)	-0.3	-	0.3	V
Vih	High level input voltage on pin.	Iih=+/-20 µA (max) with 20 k• pullup	1.19	-	1.89	V
Vil	Low level input voltage on pin.	Iil=+/-1 mA (max)	-0.3	-	0.2	V
Tr and Tf		Cin = Cout = 30 pF			1	µs
SIM_DATA_CARD at 2.8 V						
Voh	High level output voltage on pin.	Ioh=+20 µA(max)	2.2	-	3.3	V
Vol	Low level output voltage on pin.	Iol=-200 µA (max)	-0.3	-	0.6	V
Vih	High level input voltage on pin.	Iih=+/-1 µA (max) with 20 k • pullup	1.89	-	3.3	V
Vil	Low level input voltage on pin.	Iil=+1 mA (max)	-0.3	-	0.4	V
Tr and Tf		Cin = Cout = 30 pF			1	µs
SIM_CLK_CARD at 1.8 V						
Voh	High level output voltage on pin.	Ioh=20 µA (max)	1.32	-	1.89	V
Vol	Low level output voltage on pin.	Iol=-20 µA (max)	-0.3	-	0.3	V
Tr and Tf	Rise Time	Cin = Cout = 30 pF	-	-	50	ns
SIM_CLK_CARD at 2.8 V						
Voh	High level output voltage on pin.	Ioh=20 µA (max)	1.89	-	3.3	V
Vol	Low level output voltage on pin.	Iol=-200 µA (max)	-0.3	-	0.66	V
Tr and Tf		Cin = Cout = 30 pF	-	-	50	ns
Clock	Frequency		1		4	MHz
SIM_RST_CARD at 1.8 V						
Voh	High level output voltage on pin.	Ioh=20 µA (max)	1.36	-	1.89	V
Vol	Low level output voltage on pin.	Iol=-200 µA (max)	-0.3	-	0.3	V
Tr and Tf	Rise Time	Cin = Cout = 30 pF	-	-	400	µs

Table 70. SIM Interface Electrical Specifications (2 of 2)

Symbol	Parameters	Conditions	Minimum	Typical	Maximum	Units
SIM_RST_CARD at 2.8 V						
Voh	High level output voltage on pin.	Ioh=20 µA (max)	1.89	-	3.3	V
Vol	Low level output voltage on pin.	Iol=-200 µA (max)	-0.3	-	0.6	V
Tr and Tf	Rise Time	Cin = Cout = 30 pF	-	-	400	µs
HOST Side at VIO (1.8 and 2.8 V)						
SIM_DATA_HOST						
Voh	High level output voltage on pin.	Ioh=20 µA (max)	80%*V_{IO}	-	-	V
Vol	Low level output voltage on pin.	Iol=-200 µA (max)	-0.3	-	20%*V_{IO}	V
Vih	High level input voltage on pin.	Iih=20 µA (max)	80%*V_{IO}	-	-	V
Vil	Low level input voltage on pin.	Iil=1.5 mA (max)	-0.3	-	5%*V_{IO}	V
Tr and Tf		Cin = Cout = 30 pF			1	µs
SIM_CLK_HOST						
Vih	High level voltage on pin.	Iih=-20 µA (max)	80%*V_{IO}	-	-	V
Vil	Low level voltage on pin.	Iil=20 µA (max)	-0.3	-	15%*V_{IO}	V
Tr and Tf	Rise Time	Cin = Cout = 30 pF	-	-	20	ns
Clock	Frequency		1		4	MHz
SIM_RST_HOST						
Vih	High level voltage on pin.	Iih=-20 µA (max)	80%*V_{IO}	-	-	V
Vil	Low level voltage on pin.	Iil=20 µA (max)	-0.3	-	15%*V_{IO}	V
Tr and Tf	Rise Time	Cin = Cout = 30 pF	-	-	400	µs

Table 71. 19.5 MHz Crystal Specifications (1 of 2)

Parameter	Requirement	Note/Conditions
Electrical Requirements		
Mode	Fundamental	
Type	Parallel	
Drive Level	100 μW (max.)	75 μW (typical)
Load Capacitance, (C_{LD}) Range Nominal Value	 4.3 pF • C_{LD} • 10.0 pF 7.0 pF	Crystal input and output load capacitances are unequal. Load capacitance, C_{LD}, is composed of variable capacitances C_{LD1} and C_{LD2}: $C_{LD}=(C_{LD1} \times C_{LD2})/(C_{LD1} + C_{LD2})$ Assumes external capacitances due to circuit board pads & traces on crystal input and output are each less than 1.5 pF.
Nominal Resonant Frequency	19.5 MHz	C_{LD} = Nominal @ Temp = 25ºC
Frequency Accuracy/Stability		Exclusive of load capacitance:
Initial Tolerance	• ± 10 ppm	Using C_{LD} = Nominal @ Temp = 25 ºC
Drift Over Temperature	• ± 12 ppm	-30 ºC < Temp < 70 ºC
Drift due to Aging	• ± 5 ppm	Over 5 years
Crystal Parameters		
Series Resistance, R_S	• 40 Ω	Using 20 nW drive level.
Motional Capacitance, C_m Motional Inductance, L_m Shunt Capacitance, C_0	Bounded by ratios	
Pullability, PA	• 200 ppm	$PA = C_m / 2 (Co + C_{LD}) x 10^6$ ppm Using max C_{LD}, all capacitances are in pF.
Pulling sensitivity, PS	• 100 ppm/pF	$PS = C_m / 2 (Co + C_{LD})^2 x 10^6$ ppm / pF Using max C_{LD}, all capacitances are in pF.
Phase Noise, SSB Frequency Offset:		SSB: Single-sideband This specification refers to residual phase noise of the crystal only, and applies with or without vibration.
100 Hz	• -108 dBc/Hz	
1 kHz	• -136 dBc/Hz	
• 10 kHz	• -140 dBc/Hz	
Spurious	• -15 dBc	In frequency range f_n ± 1 MHz for n = 1 to 5, where n = 1 is the fundamental frequency of oscillation and n = 2, 3, 4, 5 are harmonics.

Table 71. 19.5 MHz Crystal Specifications (2 of 2)

Parameter	Requirement	Note/Conditions
Mechanical/Environmental Requirements		
Temperature Storage Operating	 -55ºC < Temp < 105ºC -30ºC < Temp < 70ºC	
Solder Temperature	245ºC (max)	
Vibration	< 0.5 ppm Frequency shift During exposure	10-500 Hz, 1.5 mm p-p, 10g p-p
Shock	< 0.5 ppm Frequency shift After exposure to shock	100g's (980m/s^2); 6 ms duration; half-sine shock pulses; 6 impacts along each of 3 perpendicular axes.
Humidity	Resistant to 95% non-condensing @ 40ºC	

Table 72. System Voltage Regulator Electrical Specifications (1 of 3)

Parameter	Conditions	Max
VIO (CL=0.33F µF Load Capacitance)		
Output Voltage (before bandgap timing)	All loads	2.80 V ± 8%
Output Voltage Accuracy	After Bandgap tuning	± 1%
Output Current	At minimum Input voltage (3.3 V)	130 mA
Drop-Out Voltage (2.8 V only)	Vd @ 50% Load	100 mV
Ground Current (Biasing)	No load (500 µA)	50 µA
Output Noise	10 to 10 kHz	50 µVrms
Power Supply Rejection Ratio	216 Hz	60 dB
VCORE (1 µF Load Capacitance)		
Output Voltage (before bandgap timing)	Controlled by VSEL0 and VSEL1	1.2 V ± 8%
Output Voltage (before bandgap timing)	Controlled by VSEL0 and VSEL1	1.7 V ± 8%
Output Voltage (before bandgap timing)	Controlled by VSEL0 and VSEL1	2.4 V ± 8%
Output Voltage (before bandgap timing)	Controlled by VSEL0 and VSEL1	2.8 V ± 8%
Output Voltage Accuracy	(after bandgap tuning for all voltages)	± 1%
Output Current	At minimum Input voltage (3.0 V)	80 mA
Drop-Out Voltage	Vd @ 50% Load (Vout = 2.8 V)	100 mV
Ground Current (Biasing)	For all loads	50 µA
Output Noise	10 Hz to 10 kHz	50 µVrms
Power Supply Rejection Ratio	216 Hz	60 dB min.
Cross-Regulator Rejection Ratio	216 Hz	60 dB min.

Table 72. System Voltage Regulator Electrical Specifications (2 of 3)

Parameter	Conditions	Maximum
VUHF (CL=0.33 µF Load Capacitance)		
Output Voltage	All loads (before bandgap tuning)	2.80 V ± 8%
Output Voltage Range	All loads	2.25 to 3.0 V
Output Voltage Accuracy	After Bandgap tuning	± 1%
Output Voltage Adjustment step size	All loads	50 mV
Output Current	At minimum Input voltage (3.0 V)	50 mA
Drop-Out Voltage	Vd @ 50% Load	100 mV
Ground Current (Biasing)	For all loads (overload ON)	500 µA
Ground Current (Biasing)	For all loads (overload OFF)	250 µA
Output Noise	10 to 10 kHz	50 µVrms
Power Supply Rejection Ratio	216 Hz	60 dB
VRF (1 µF Load Capacitance)		
Output Voltage	All loads (before bandgap tuning)	2.80 V ± 8%
Output Voltage Range	All loads	2.25 to 3.0 V
Output Voltage Accuracy	After Bandgap tuning	± 1%
Output Voltage Adjustment step size	All loads	50 mV
Output Current	At minimum Input voltage (3.0 V)	150 mA
Drop-Out Voltage	Vd @ max. Load	100 mV
Ground Current (Biasing)	For all loads (overload ON)	500 µA
Ground Current (Biasing)	For all loads (overload OFF)	250 µA
Output Noise	10 to 10 kHz	50 µVrms
Power Supply Rejection Ratio	216 Hz	60 dB
VTIC (CL=0.33 µF Load Capacitance)		
Output Voltage	All loads (before bandgap tuning)	2.80 V ± 8%
Output Voltage Range	All loads	2.25 to 3.0 V
Output Voltage Accuracy	After Bandgap tuning	± 1%
Output Voltage Adjustment step size	All loads	50 mV
Output Current	At minimum Input voltage (3.0 V)	100 mA
Drop-Out Voltage	Vd @ 50% Load	100 mV
Ground Current (Biasing)	For all loads (overload ON)	500 µA
Ground Current (Biasing)	For all loads (overload OFF)	250 µA
Output Noise	10 to 10 kHz	50 µVrms
Power Supply Rejection Ratio	216 Hz	60 dB
VSIM (1.8 V Mode) (CL=0.10 µF Load Capacitance)		

Output Voltage	1.8 Volt Mode	1.80V ± 3%
Output Current	At Minimum Input voltage (3.0V)	10mA
Line Regulation	From Vin_{min} to Vin_{max}	0.75%/V
Load Regulation	1mA to full load (10.0mA)	10mV
Quiescent Current	Regulator OFF state	1μA
Ground Current (Biasing)	No load (100uA)	50uA
Output Noise	10 to 10KHz	100μVrms
Power Supply Rejection Ratio	216Hz	60dB
Enable Response Time	To be within 3% of V_o, C_L=1.0μF	250μs

Note*. For 3 V SIM mode, 1.8 V regulator is shut down (supply voltage comes from the V10 regulator.*

Table 72. System Voltage Regulator Electrical Specifications (3 of 3)

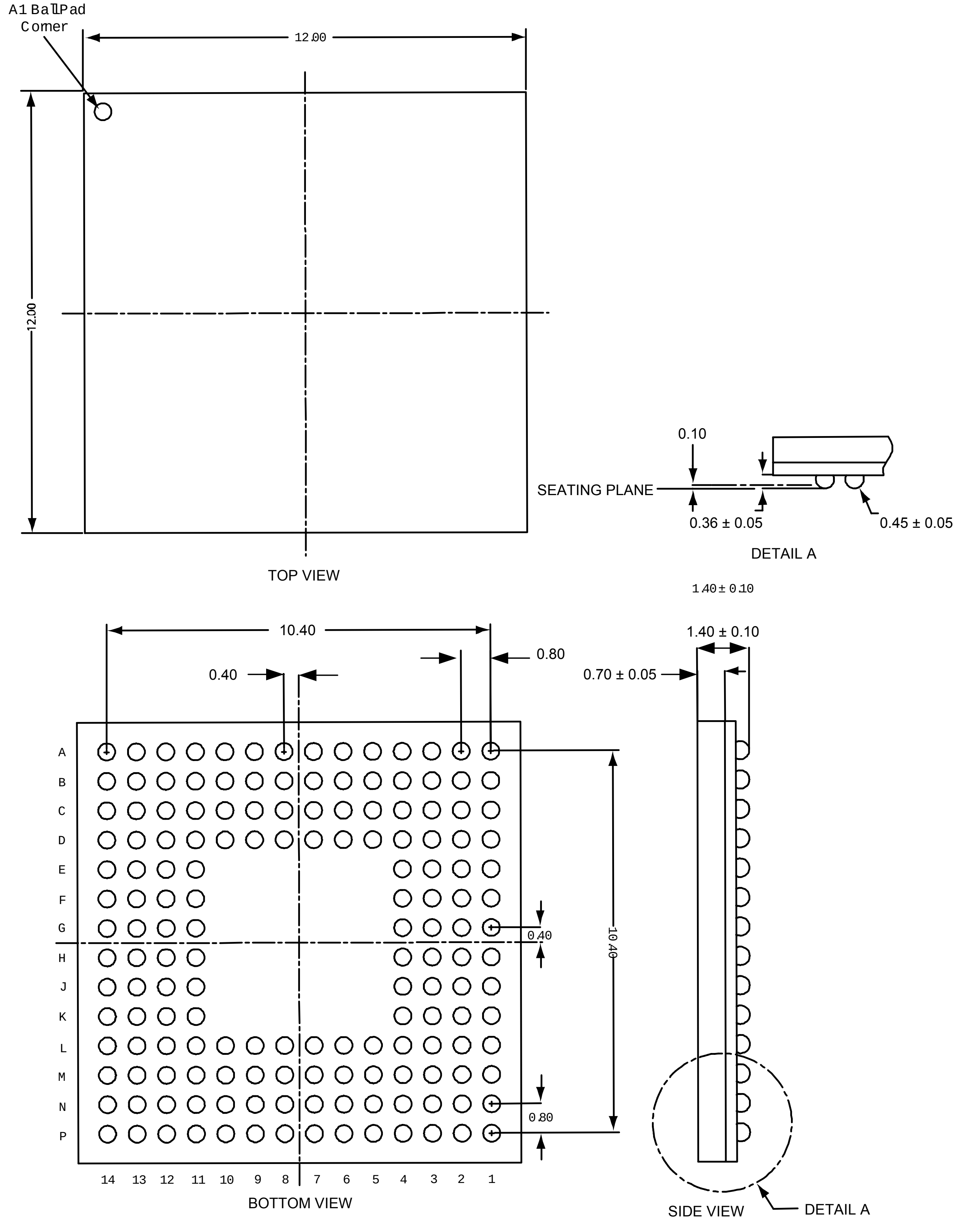
Parameter	Conditions	Maximum
Internal Analog Regulator (CL=0.01 µF)		
Input voltage		5.5 V
Default output regulated voltage	load = 0	2.825 V ± 2%
	Max load	> 2.7V
Drop-out voltage	Max load	63 mV
Output noise	1 kHz to 100 kHz	80 µV
Power supply rejection ratio	216 Hz	70 dB
Cross regulator rejection	216 Hz	80 dB
Ground current	For all loads	135 µA
Output current VD1/VD2 VCODEC VA1 VA2 VXTAL VAUX1 VAUX2 VAUX3 VAUX4	For all loads	 5 mA 48 mA 25 mA 12 mA 5 mA 12 mA 5 mA 5 mA 25 mA
VRTC Pre-LDO		
Output voltage	All loads	3.3V ±10%
Output current	At Minimum Input voltage	250 µA
Ground current (Biasing)	No load	10 µA
Tcharge	Time required to fully charge a 100 µF capacitor.	1 sec.
VBATTERY – VBackup comparator hystersis		205 ± 60 mV
VRTC LDO (C_L=0.01µF)		
Output Voltage High	All loads	1.2 V ±10%
Output Voltage Medium	All loads	1.7 V ±10%
Output Voltage Low	All loads	2.4 V ±10%
Output Current	At Minimum Input voltage	20 µA
Ground Current (Biasing)	Full load	20 µA

Table 73. Reference Voltages

Pin Name	Value	Load
VC_XTAL	1.35 V	0.1 µF
VC_REF+	1.85 V	
VC_REF-	0.85 V	
VC	1.35 V	
VC_CODEC	1.35 V	
MIC_CAP	2.2 V	
MIC_BIAS	~2 V	
RBIAS	1.2 V	1 %

Table 74. Sleep Mode Active Functions

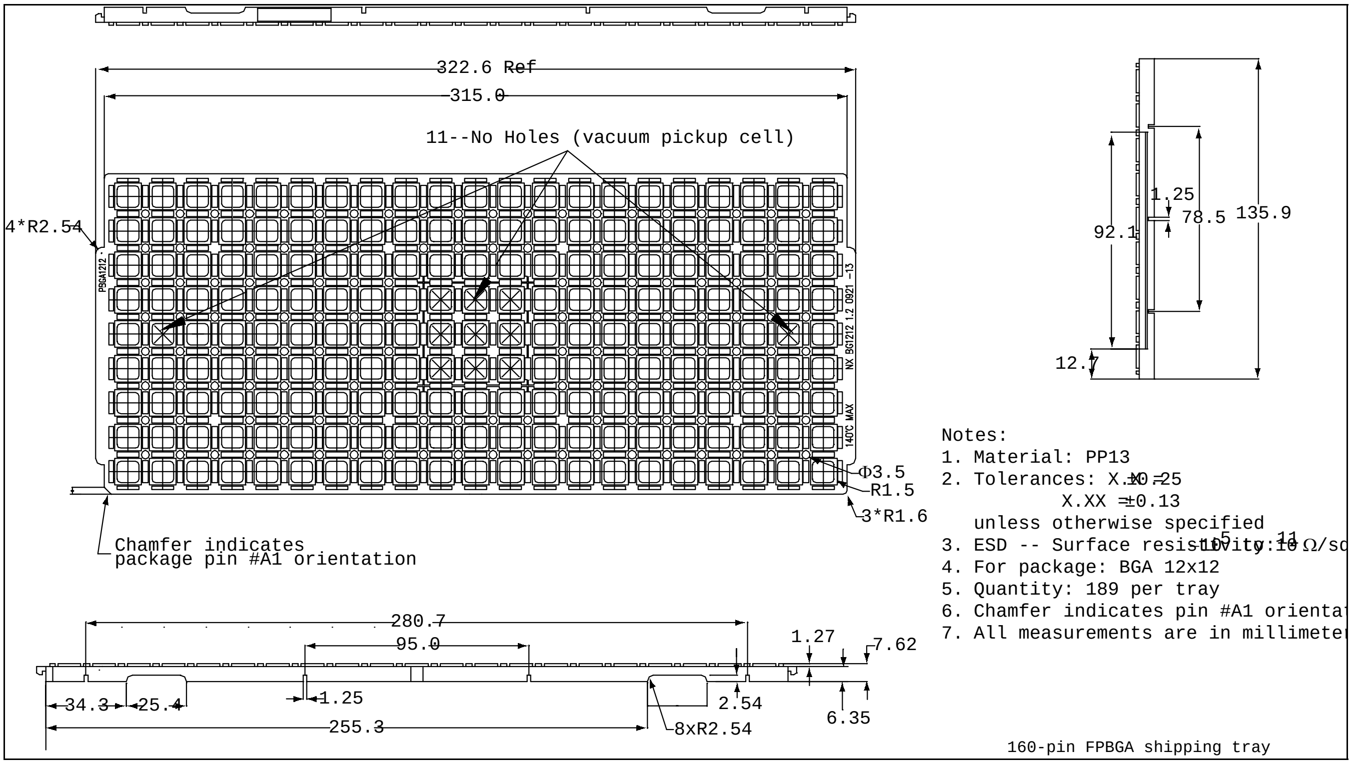
Function/Pins	States/Actions
VCORE	ON/no resistive load (all voltages)
VIO (2.8 V)	ON/no resistive load
VRF	OFF (EN_1,2 & 3 Low)
VUHF	OFF (EN_1,2 & 3 Low)
VTIC	OFF (EN_1,2 & 3 Low)
VSIM	ON, 2.8 V, no load
VRTC	ON and connect 330 k• to ground
BACKUP	Connect 0.01 µF Capacitor to ground, no resistive load
VCHARGE	OFF (VCHARGE Low)
MUX_OUT	Write 00h in register 0Ch
DTR	Float
ALARM	Pulled to VRTC
PWR_KEY_L	Pulled to VPOWER
PWR_KEY_H	Grounded
SIM_EN	High
SIM_DATA_HOST	High
SIM_CLK_HOST	Low
SIM_RST_HOST	High
SERIAL_DATA	High
SERIAL_CLOCK	High
MSD_RESET	High
CLK_REQ	Low
BAT_PK_IN	Float
VSEL0 and VSEL1	Grounded



All dimensions are in millimeters

160-Pin FPBGA Package Dimensions

Figure 25. 160-Pin FPBGA Package Dimensions



Notes:
1. Material: PP13
2. Tolerances: X.X = ±0.25
X.XX = ±0.13
unless otherwise specified
3. ESD -- Surface resistivity: 10^5 - 10^{11} Ω/sq
4. For package: BGA 12x12
5. Quantity: 189 per tray
6. Chamfer indicates pin #A1 orienta
7. All measurements are in millimete

Figure 26. 160-Pin FPBGA Shipping Tray

Complete Pegasus GSM/GPRS System Solution Ordering Information

Table 75 lists the technical documentation, part number, and ordering information for the CX20524 and the Complete GSM/GPRS System Solution.

Table 75. Ordering Information

Data Sheet		Pegasus Product Number	Part Number	Software Code Version	Title/Description
Number	Date				
102019B (current document)	July 12, 2002	CX20524	TBD	TBD	Mixed Signal Device for GSM and GPRS Applications

Note.*Consult with a Skyworks Product Application Engineer to ensure that you obtain the most current revision of a Data Sheet. Revisions are signified by a letter designation after the Data Sheet Number (for example: 123456A).*

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