

Single Chip Engine (SCE200)

Device Set

The Conexant™ Single Chip Engine (SCE) Device Set consists of a FAX Controller combined with an embedded modem Digital Signal Processor (DSP), an embedded SmartDAA IF, and a separate SmartDAA device.

This device set, along with the supporting firmware and evaluation system, comprise a complete facsimile machine—needing only power supply, scanner, and printer mechanism components to complete the machine. A system-level block diagram is shown in Figure 1.

Integrated SCE Controller

The integrated SCE controller (SCC) provides the majority of the electronics necessary to build a thermal or thermal transfer facsimile machine integrated into a one-chip solution. The controller performs primary facsimile control/monitoring and compression/decompression functions, interfaces with fax machine components such as a scanner, printer, motor, and operator control panel. The MC24 embedded processor provides an external 16 MB direct memory access capability. An integrated Pipeline ADC, combined with Conexant's Image Processing Scheme, provides state of the art image processing performance on text and gray scale images.

Embedded Modem DSP

The SCE embedded modem DSP supports V.29 and V.27 ter facsimile transmission and reception, in addition to all basic HDLC functions and T.30 requirements. The modem allows all line connections and single or dual tone generation and detection. Optional features such as V.17, voice compression/decompression for Digital Telephone Answering Machine (DTAM), and duplex speakerphone are also available.

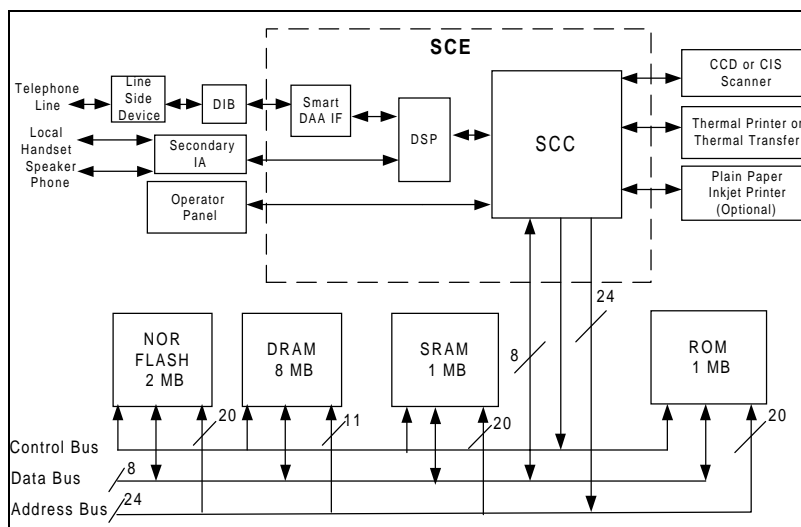


Figure 1. Single Chip Engine - SCE200

Features

- Microprocessor and Bus Interface
 - MC24 central processing unit (CPU)
 - 8.064 MHz CPU clock speed
 - Memory efficient input/output bit manipulation
 - 24-bit internal address bus, 8-bit data bus
- External Bus
 - Address, data, control, status, and decoded chip select signals support connection to external ROM, SRAM, DRAM and operator panel
 - 24-bit external address bus
 - 8-bit data bus
- Chip selects
 - ROMCSn for ROM support
 - CS0n for SRAM
 - FCSn for FLASH memory support
 - LCDCS for LCD support
- DRAM Controller
 - Up to 8 MB supported in two blocks
 - Organizations supported: 4 or 8-bit
 - Single and page mode access support
- Flash memory support
 - NAND and NOR type support
 - Serial NAND support
 - NOR type memory up to 2 MB
- DMA Controller
 - Six dedicated internal DMA channels for scanner, T.4/T.6, and printer access
- Moveable external SRAM memory (covered by CS0n) up to 1 MB
- External ROM memory (covered by ROMCSn) up to 1 MB
- Internal Interrupt controller
- T.4/T.6 Compression and Decompression in hardware
 - MH/MR
 - MMR
 - Alternating Compression/Decompression
- Scanner/Printer Stepper Motor Control
 - Four outputs to external current drivers for the scanner stepper motor
 - Four outputs to external current drivers for the printer stepper motor
 - Programmable for acceleration/deceleration

- Scanner and Video Control
 - CIS or CCD scanners supported
 - Six programmable control signals
 - B4/A4 scanner support
 - 5 ms minimum line time
 - Line lengths up to 4096 pixels
 - Embedded scanner pipeline A/D
 - Built-in Programmable Clamping, Analog Gain Control, and Sample/Hold circuits
- Video Processing
 - Two modes of shading correction
 - Dark level correction
 - Gamma correction and MTF
 - 2-D Error Diffusion or Dithering
 - Multi-level B4-A4 fixed resolution conversion
- Bi-Level Resolution Conversion
 - Programmable bi-level resolution conversion block provides expansion or reduction on the T.4/T.6 decompressed data or scan image data
 - Programmable image expansion up to 200% or reduction down to 60%
 - Vertical line ORing
- Printer interface supports thermal or thermal transfer printers
- Optional plain paper inkjet printer support
- Dedicated interface to support operator panel
 - 32 key direct support
 - 8 LED direct support
 - LCD support
- Two Synchronous Interface (SSIF)
- Synchronous/Asynchronous Interface (SASIF)
- Programmable Tone Generator
 - Frequency and output levels are programmable
- General Purpose Inputs/Outputs
 - 38 GPIO and 32 GPO lines are provided
- Embedded modem DSP
 - Supports speeds up to 9600 bps and V.21 Channel 2 transmission/reception
 - Supports HDLC framing and detection
 - Supports DTMF generation/reception
 - Supports CID reception
 - Optional V.17 (14.4 Kbps)
- SmartDAA Technology
 - Digital Isolation Barrier (patent pending)
 - Integrated DAA and IA function
 - Worldwide PTT regulation tested
- Optional DTAM support
 - V24 24 minutes of voice storage per 4 Mbits of memory
 - ADPCM codec
 - PCM codec
 - Near-end echo cancellation
- Optional duplex Speakerphone
 - Speakerphone IA support
 - Acoustic Echo Cancellation
 - Line Echo Cancellation or Secondary Acoustic Echo Cancellation
- Real-Time Clock with Battery Backup
- Programmable Watchdog Timer
- EMI reduction on pads
- Stand-by and Sleep modes to reduce power consumption
- On-chip or off-chip Power Up/Down detection
- 3.3 V operation
- 3.3 V and 5 V compatible interface
- Compact packages
 - SCC: 176-pin TQFP
 - SmartDAA: 32-pin TQFP (not shown)
- Modular SCE Firmware
 - Real-time multitasking environment
- Fax transmit, receive, and copy
 - T.30 protocol
 - T.4/T.6 compression and decompression hardware support and control
 - Image expansion or reduction
 - Page memory functions
 - Call progress support
 - Caller ID support
- Versatile Evaluation System
 - Provides demonstration, development and evaluation capabilities
- MC24 software development tool kit

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Embedded SmartDAA IF

The SCE embedded SmartDAA IF logic provides the data path between the modem DSP and the external Conexant SmartDAA device through the Digital Isolation Barrier (DIB) and the control/status path between the MC24 CPU and the SmartDAA device. The SmartDAA IF also contains ring decoder logic which performs preliminary ring detection.

Digital Telephone Answering Machine (DTAM)

The DTAM option supports digital answering machine functionality by providing a low bit rate voice codec that provides 24 minutes of voice storage per 4 Mbits of memory.

Speakerphone

The Speakerphone option adds duplex digital speakerphone capability for hands-free applications. An additional Integrated Analog (IA) front-end is required for microphone and speaker interface to support duplex digital speakerphone operation.

SCE Evaluation System (FEES-SCE)

The SCE Evaluation System provides demonstration, prototype development, and evaluation capabilities to facsimile machine developers using the SCE device set. In addition, it provides a plug-on board for the operator panel, sockets for programmable parts, and connectors for an emulator. The operator panel on the SCE Evaluation System allows for complete control and monitoring of functions. All necessary sockets for memory components are included. Jumper options and test points are provided throughout the SCE board.

The SCE Evaluation System is the most convenient environment for the developer needing to experiment with the various interfaces encountered in a fax machine. The SCE Evaluation System along with SCE hardware and SCE application code, comprise a working facsimile machine.

SCE Software Development Tools

The MC24 Software Development Kit (SDK) (McFERE2, 2500AD MC24 Macro Assembler, Linker, and Librarian) is available to support software/firmware development.

This package can operate under the MS-DOS, Microsoft Windows 3.x, and Windows 95 Operating Systems. This versatility provides the developer with extensive tools for code modifications and debugging.

Hardware Description

Integrated SCE Controller (SCC)

The SCE Controller contains an internal MC24 Processor with a 16 MB address space and dedicated circuitry optimized for facsimile image processing and monitoring and for thermal or thermal transfer printer support.

The CPU provides fast instruction (up to 10 MHz clock speed) execution and memory efficient input/output bit manipulation. The CPU connects to other internal SCE functions over an 8-bit data bus and 24-bit address bus and dedicated control lines.

The 24-bit external address bus, 8-bit data bus, control, status, and decoded chip select signals support connection to external ROM, SRAM, DRAM, and FLASH memory.

DRAM Controller

The SCE includes a DRAM controller with single and page mode access support which supports fast, normal, or slow refresh time. DRAM memory space is divided into two blocks, up to 4 MB each. A maximum of 8 MB of DRAM is supported. Each block has a programmable size and starting address. Refresh is performed automatically and is supported in Sleep and Stand-by modes. CAS and RAS signal support is provided for two DRAM banks for both 4-bit and 8-bit organizations. Access speeds from 50 ns to 70 ns can be supported. The DRAM controller provides battery backup refresh using DRAM battery power.

DMA Channels

Six internal DMA channels support memory access for scanner, T.4/T.6, and resolution conversion. DMA Channel 2 can be reprogrammed for external access to support thermal printing, thermal transfer, or plain paper inkjet printing.

External RAM and ROM

Moveable and programmable size external SRAM memory of up to 1 MB, DRAM memory of up to 8 MB, and ROM of up to 1 MB can be directly connected to the SCE. By using an external address decoder or CS[5]n, the size of SRAM or ROM can be extended up to 1 MB. The ROM stores all the SCE program object code. SRAM is used by the SCE Embedded CPU for shading RAM, image line buffer RAM, and ECM buffer.

Flash Memory Controller

The SCE includes a flash memory controller that supports NOR, NAND, and Serial NAND-type flash memory. The supported size of NOR-type memory is up to 2 MB and the supported size of NAND-type memory is unlimited.

Stepper Motor Control

Eight outputs are provided to external current drivers: four to the scanner motor and four to the printer motor. The stepping patterns are programmable and selectable line times are supported. A timeout circuit controls the power control of the motors. The printer or scanner motor outputs can be programmed as GPOs for applications using single motor or plain paper printers.

T.4/T.6 Compressor/Decompressor

MH, MR, and MMR compression and decompression are provided in hardware. T.4 line lengths of up to 4096 pixels are supported in bi-level and gray scale dithering mode. MMR and Alternating Compression/Decompression (ACD) on a line by line basis provide support for up to three independent compression and decompression processes.

Bi-level Resolution Conversion

One independent programmable bi-level 1D-resolution conversion block is provided to perform expansion or reduction on the T.4 decompressed data and scan image data. Image expansion can be programmed up to 200% and reduction down to 60%. Vertical line ORing and data output bit order reversal is also provided.

Printer IF

The Printer Interface provides a standard connection between the SCE and a thermal printhead to support thermal printing or thermal transfer. The thermal printer interface consists of programmable data, latch, clock, and up to 4 strobe signals. Programmable timing supports traditional thermal printers, as well as the latchless split mode printers, and line lengths of up to 2048 pixels. Line times from 5 ms to 40 ms are supported.

The SCE includes a thermal ADC (TADC) function utilizing a D/A converter and a comparator to monitor the printhead temperature. External terminating resistors must be supplied; the values are determined by the specific printhead selected. As an option, plain paper inkjet printing can be supported.

Scanner and Video Control

Six programmable control and timing signals support common CCD and CIS scanners. The video control function provides signals for controlling the scanner and for processing its video output. Four programmable control signals (START, CLK1, CLK1n, and CLK2) provide timing related to line and pixel timing. These are programmable with regard to start time, relative delay and pulse width.

Two video control output signals (VIDCTL[1:0]) provide digital control for external signal pre-processing circuitry. These signals provide a per pixel period, or per line period, timing with programmable duration and polarity control for each signal.

Scanner Pipeline A/D Interface

An internal 8-bit Pipeline A/D converter (PADC) is provided. The A/D reference input (+Vref) is externally fixed to VDD. Internal +Vref is available for control by the CPU. The internal +Vref covers the range from +2.25 V to +2.7 V. Scanner input signal supported with full scale is from 0.65 V P-P to 2.7 V P-P. Clamping, AGC, and Sample/Hold circuits are built-in the device.

The PADC data output includes an overflow bit. The AGC gain is programmable from 0 to 12 dB, in 1 dB steps.

Video Processing

The SCE supports two modes of shading correction for scanner data non-uniformity arising from uneven sensor output or uneven illumination. Correction is provided on either an 8-pixel group or is applied separately to each pixel. Dark level correction and gamma correction are also provided.

Two-dimensional Error Diffusion/Dithering is performed on halftone images. The SCE includes an 8 x 8 dither table, which is programmable and stored internally (8-bits per table entry). The table is arranged in a matrix of 8 rows by 8 columns. The video processing circuit provides mixed-mode detection/processing and multi-level Resolution Conversion for the scanner multi-level data. The conversion ratio of the multi-level Resolution Conversion is fixed to B4-A4 conversion.

Operator Panel Interface

Operator Panel functions are supported by the operator output bus OPO [7:0], the operator input bus OPI [3:0], and two control outputs (LCDCS and LEDCTRL).

The SCE can directly interface to a 32-key keypad. External blocking diodes are required to isolate the keyboard strobe lines from the LED's, as the LED's and keyboard strobe signals use the same lines. Up to 8 x 15 keyboard array can be supported with external circuitry.

Up to 8 LED's can be directly driven by the SCE. To prevent the dim LED glow that keyboard strobing would cause, an LED control signal is provided to disable the LED's during keyboard strobing. A 2-line LCD display module with 20 characters per line can be supported.

Synchronous Serial Interface (SSIF)

Two Synchronous only Serial Interface (SSIF) are built into the SCE, which allows the SCE to communicate with external peripherals. Each SSIF provides separate signals for Data (SSTXD, SSRXD), Clock (SSCLK), and Status (SSSTAT). Each SSIF is a full duplex, three-wire system. The SSIF may be configured to operate as either a master or slave interface. The bit rate, clock polarity, clock phase, and data shifting order are programmable.

Synchronous/Asynchronous Serial Interface (SASIF)

One Synchronous/Asynchronous Serial Interface (SASIF) performs the following:

- Serial-to-parallel conversion of data received from a peripheral device
- Parallel-to-serial conversion of data for transmission to a peripheral device.

This interface consists of serial transmit data (SASTXD), serial receive data (SASRXD), and a serial clock (SASSCLK). The SASIF includes a programmable bit rate generator for asynchronous and synchronous operations. The data shifting order, data bit number, and the SASSCLK polarity are programmable.

Real-Time Clock (RTC)

The SCE includes a battery backup real-time clock. The RTC will automatically maintain the proper date and time for 32 years. Leap year compensation is included. A 32.768 KHz or 65.536 KHz crystal is required by the RTC.

Tone Generator

The SCE provides a programmable tone generator output. The frequency of the tone generator is programmable from 400 Hz to 4 KHz. By using a PWM programmable high frequency as a modulation frequency, the output level can be made programmable.

Watchdog Timer

The programmable Watchdog Timer is intended to guard against firmware lockup on the part of either executive-controlled background tasks or interrupt-driven tasks, and can only be enabled by a sequence of events under control of the Watchdog Control logic. Once the Watchdog Timer has been enabled, it can not be disabled unless a system reset occurs.

Reset and Power Control

The RESETn I/O pin provides an internally-generated reset output signal to external circuits, or it can accept an externally-generated reset signal. This reset signal will not reset the RTC. Separate RTC battery power inputs are provided for battery-backup functions. A BATRSTn pin is provided, which resets the RTC circuits and all other SCE circuits.

Power Up/Down Control

Power Up/Down detection is provided internally. The threshold voltages are:

- Power Up detection level = $2.9\text{ V} \pm 50\text{ mV}$
- Hysteresis = 20 mV

An internally generated power down signal controls internal switching between primary and battery power. This control signal is also provided as an output on the PWRDWNn pin. An externally generated power down detector (optional) can be provided as an input on the PWRDWNn pin by setting the INTPWRDWNEn pin. The minimum power up detection is 2.85 V with power down detection at 2.83 V. The maximum power up detection is 2.95 V with power down detection at 2.93 V.

Stand-by and Sleep Modes

Two power saving modes are provided to reduce the power consumption. In Stand-by mode, the CPU is functional, however the modem clock is turned off to save power. When this occurs, the modem may be activated by software under different conditions. In Sleep mode, the clock is cut off from both the modem and the CPU to increase the power savings. The DRAM refresh is still functional. The system can be activated by paper insertion, key pressing events, or telephone ring detection.

Embedded Modem DSP

The embedded modem DSP is a synchronous 9600 bps (14400 bps optional) half-duplex modem with error detection/reception. It provides data transmission/reception from regular PSTN lines, PBX, or private lines. The modem can operate at any standard V.29 data speed up to 9600 bps as well as in V.21 and V.23 modes.

The modem is designed for use in Group 3 facsimile machines and satisfies the requirements specified in ITU-T Recommendations V.29, V.27 ter, V.21 Channel 2, and T.4, and meets the signaling requirements of T.30. It also performs HDLC framing according to T.30 at all speeds.

SmartDAA Features

- Eliminates traditional expensive discrete DAA components
- Reduces the number of modem and DAA components for smaller mobile/notebook designs
- Reduces modem and DAA board footprint to less than 1/3 the area of traditional DAA designs
- Allows common hardware designs for international application
- World-wide homologation – single board design can achieve approval for world-wide shipments
- FCC- and world-wide compliant connections to the analog PSTN/GSTN
- World-wide usage – with the right cable, the mobile user can use anywhere
- Digital isolation – lower floor noise allows higher connect rates
- Digital PABX protection – protects mobile use from high voltage PABX lines
- Software selectable Ring Detect – supports wake-on-ring
- Detect remote hang-up – for efficient call termination
- System Side Powered DAA
- Pulse dialing

Software and Firmware Support Features

Available software and embedded firmware provides the following:

- Modem support for speeds up to 9600 bps (14400 bps optional)
- ECM under conditional assembly
- DRAM memory support under conditional assembly
- MH, MR and MMR support
- Page memory receiving
- 5 ms minimum scan line time
- Conditional Error Diffusion or Dither table (8x8) support
- Dark Level Correction support
- Single motor support
- 32-key operator panel support
- Call progress support for Europe and US
- Monochrome inkjet print engine support

SCE Pin Assignments and Signal Definitions

The SCE 176-pin TQFP signals are shown in Figure 2 and listed in Table 1.

Power Requirements

Power requirements are listed in Table 2.

Absolute Maximum Ratings

Absolute maximum ratings are listed in Table 3.

Crystal Specifications

The crystal specifications are listed in Table 4.

Package Dimensions

The 176-pin TQFP package dimensions are shown in Figure 3.

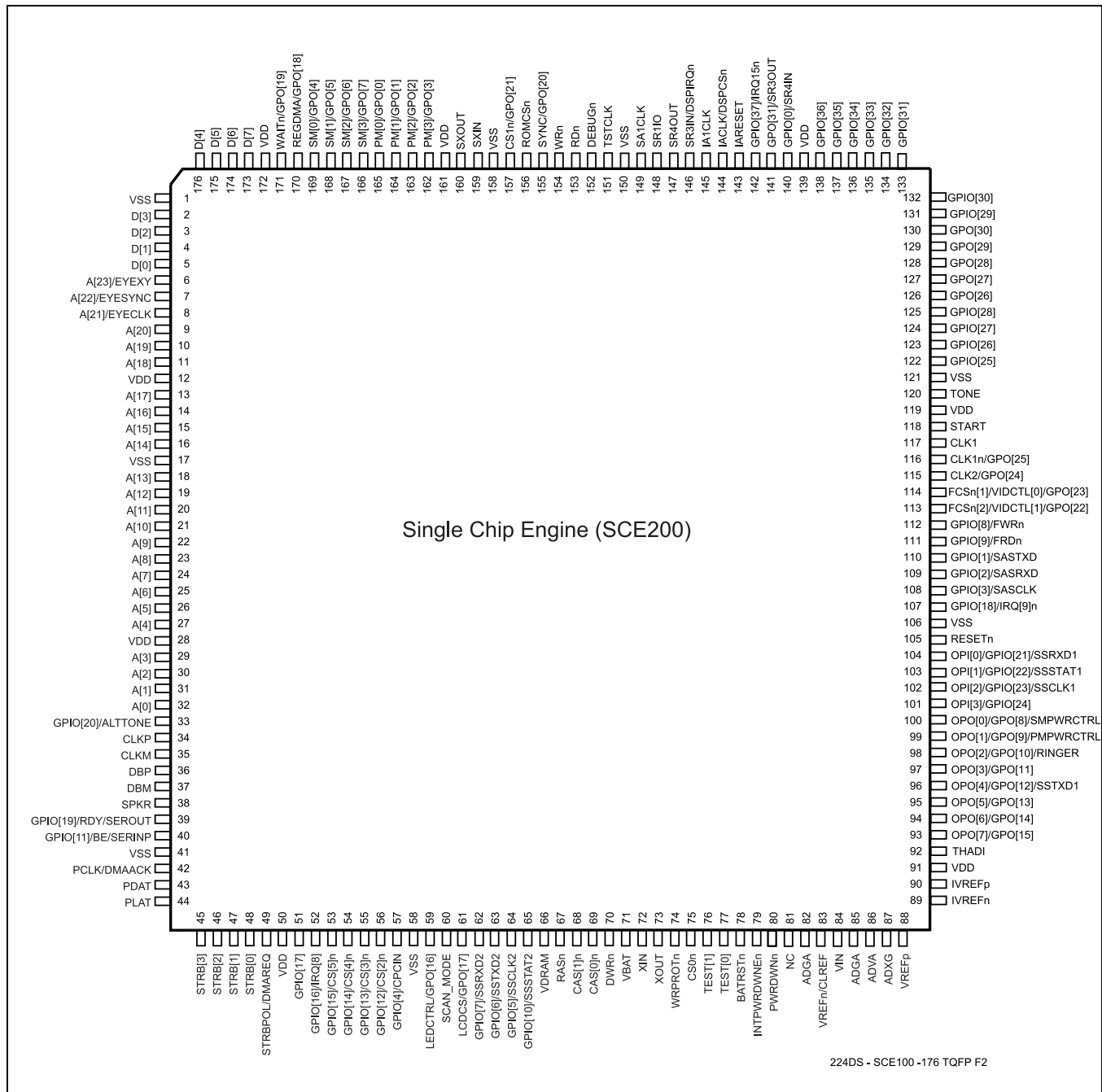


Figure 2. SCE 176-Pin TQFP Signals

Table 1. SCE 176-Pin TQFP Assignments

Pin	Signal Label	I/O	Input Type	Output Type	Pin Description
1	VSS	—	—	—	VSSi
2	D[3]	I/O	Tu	13Xs	CPU Data Bus
3	D[2]	I/O	Tu	13Xs	CPU Data Bus
4	D[1]	I/O	Tu	13Xs	CPU Data Bus
5	D[0]	I/O	Tu	13Xs	CPU Data Bus
6	A[23]/EYEXY	I/O	Tu	13Xs	CPU Address Bus
7	A[22]/EYESYNC	I/O	Tu	13Xs	CPU Address Bus
8	A[21]/EYECLK	I/O	Tu	13Xs	CPU Address Bus
9	A[20]	I/O	Tu	13Xs	CPU Address Bus
10	A[19]	I/O	Tu	13Xs	CPU Address Bus
11	A[18]	I/O	Tu	13Xs	CPU Address Bus
12	VDD	—	—	—	VDDo
13	A[17]	I/O	Tu	13Xs	CPU Address Bus
14	A[16]	I/O	Tu	13Xs	CPU Address Bus
15	A[15]	I/O	Tu	13Xs	CPU Address Bus
16	A[14]	I/O	Tu	13Xs	CPU Address Bus
17	VSS	—	—	—	VSSo
18	A[13]	I/O	Tu	13Xs	CPU Address Bus
19	A[12]	I/O	Tu	13Xs	CPU Address Bus
20	A[11]	I/O	Tu	13Xs	CPU Address Bus
21	A[10]	I/O	Tu	13Xs	CPU Address Bus
22	A[9]	I/O	Tu	13Xs	CPU Address Bus
23	A[8]	I/O	Tu	13Xs	CPU Address Bus
24	A[7]	I/O	Tu	13Xs	CPU Address Bus
25	A[6]	I/O	Tu	13Xs	CPU Address Bus
26	A[5]	I/O	Tu	13Xs	CPU Address Bus
27	A[4]	I/O	Tu	13Xs	CPU Address Bus
28	VDD	—	—	—	VDDi
29	A[3]	I/O	Tu	13Xs	CPU Address Bus
30	A[2]	I/O	Tu	13Xs	CPU Address Bus
31	A[1]	I/O	Tu	13Xs	CPU Address Bus
32	A[0]	I/O	Tu	13Xs	CPU Address Bus
33	GPIO[20]/ALTTONE	I/O	Hu	13Xs	—
34	CLKP	0	—	Analog	SDAA CLK +
35	CLKM	0	—	Analog	SDAA CLK -
36	DBP	I/O	Analog	Analog	SDAA DATA +
37	DBM	I/O	Analog	Analog	SDAA DATA -
38	SPKR	0	—	1XC	SDAA Speaker Output
39	GPIO[19]/RDY/SEROUT	I/O	Hu	13Xs	—
40	GPIO[11]/BE/SERINP	I/O	Hu	13Xs	—
41	VSS	—	—	—	VSSi
42	PCLK/DMAACK	0	—	3XC	—
43	PDAT	0	—	2XC	—
44	PLAT	0	—	3XC	—

Table 1. SCE 176-Pin TQFP Assignments (Cont'd)

Pin	Signal Label	I/O	Input Type	Output Type	Pin Description
45	STRB[3]	0	—	1XC	—
46	STRB[2]	0	—	1XC	—
47	STRB[1]	0	—	1XC	—
48	STRB[0]	0	—	1XC	—
49	STRBPOL/DMAREQ	I	H	—	—
50	VDD	—	—	—	VDDo
51	GPIO[17]	I/O	Hu	13Xs	—
52	GPIO[16]/IRQ[8]	I/O	Hu	13Xs	—
53	GPIO[15]/CS[5]n	I/O	Hu	13Xs	—
54	GPIO[14]/CS[4]n	I/O	Hu	13Xs	—
55	GPIO[13]/CS[3]n	I/O	Hu	13Xs	—
56	GPIO[12]/CS[2]n	I/O	Hu	13Xs	—
57	GPIO[4]/CPCIN	I/O	Hu	13Xs	—
58	VSS	—	—	—	VSSo
59	LEDCTRL/GPO[16]	0	—	4XC	—
60	SCAN_MODE	I	Hd	—	—
61	LCDCS/GPO[17]	0	—	1XC	—
62	GPIO[7]/SSRXD2	I/O	Hu	13Xs	—
63	GPIO[6]/SSTXD2	I/O	Hu	13Xs	—
64	GPIO[5]/SSCLK2	I/O	Hu	13Xs	—
65	GPIO[10]/SSSTAT2	I/O	Hu	13Xs	—
66	VDRAM	—	—	—	VDDio
67	RASn	0	—	13Xs	—
68	CAS[1]n	0	—	13Xs	—
69	CAS[0]n	0	—	13Xs	—
70	DWRn	0	—	13Xs	—
71	VBAT	—	—	—	VDDio
72	XIN	I	Osc1	—	—
73	XOUT	0	—	Osc1	—
74	WRPROTn	0	—	1XC	—
75	CS0n	0	—	13Xs	—
76	TEST[1]	I	Hd	—	—
77	TEST[0]	I	Hd	—	—
78	BATRSTn	I	H	—	—
79	INTPWRDWNEn	I	H	—	—
80	PWRDWNn	I/O	H	13Xs	—
81	NC	—	—	—	Reserved
82	ADGA	—	VADG	—	PADC
83	VREFn/CLREF	I	VR-	—	PADC
84	VIN	I	VA	—	PADC
85	ADGA	—	VADG	—	PADC
86	ADVA	—	VADV	—	PADC
87	ADXG	—	VXG	—	PADC
88	VREFp	I	VR	—	PADC

Table 1. SCE 176-Pin TQFP Assignments (Cont'd)

Pin	Signal Label	I/O	Input Type	Output Type	Pin Description
89	IVREFn	I	VR-	—	PADC
90	IVREFp	I	VR+	—	PADC
91	VDD	—	—	—	VDDi
92	THADI	I	Analog	—	TADC
93	OPO[7]/GPO[15]	O	—	13Xs	—
94	OPO[6]/GPO[14]	O	—	13Xs	—
95	OPO[5]/GPO[13]	O	—	13Xs	—
96	OPO[4]/GPO[12]/SSTXD1	O	—	13Xs	—
97	OPO[3]/GPO[11]	O	—	13Xs	—
98	OPO[2]/GPO[10]/RINGER	OZ	—	13Xs	—
99	OPO[1]/GPO[9]/PMPWRCTRL	O	—	13Xs	—
100	OPO[0]/GPO[8]/SMPWRCTRL	O	—	13Xs	—
101	OPI[3]/GPIO[24]	I/O	Hu	13Xs	—
102	OPI[2]/GPIO[23]/SSCLK1	I/O	Hu	13Xs	—
103	OPI[1]/GPIO[22]/SSSTAT1	I/O	Hu	13Xs	—
104	OPI[0]/GPIO[21]/SSRXD1	I/O	Hu	13Xs	—
105	RESETn	I/O	Hu	2XC	—
106	VSS	—	—	—	VSSo
107	GPIO[18]/IRQ[9]n	I/O	Hu	13Xs	—
108	GPIO[3]/SASCLK	I/O	Hu	13Xs	—
109	GPIO[2]/SASRXD	I/O	Hu	13Xs	—
110	GPIO[1]/SASTXD	I/O	Hu	13Xs	—
111	GPIO[9]/FRDn	I/O	Hu	13Xs	—
112	GPIO[8]/FWRn	I/O	Hu	13Xs	—
113	FCSn[2]/VIDCTL[1]/GPO[22]	O	—	13Xs	—
114	FCSn[1]/VIDCTL[0]/GPO[23]	O	—	13Xs	—
115	CLK2/GPO[24]	O	—	13Xs	—
116	CLK1n/GPO[25]	O	—	13Xs	—
117	CLK1	O	—	2XC	—
118	START	O	—	2XC	—
119	VDD	—	—	—	VDDo
120	TONE	O	—	Analog	—
121	VSS	—	—	—	VSSi
122	GPIO[25]	I/O	Hu	13Xs	—
123	GPIO[26]	I/O	Hu	13Xs	—
124	GPIO[27]	I/O	Hu	13Xs	—
125	GPIO[28]	I/O	Hu	13Xs	—
126	GPO[26]	O	—	13Xs	—
127	GPO[27]	O	—	13Xs	—
128	GPO[28]	O	—	13Xs	—
129	GPO[29]	O	—	13Xs	—
130	GPO[30]	O	—	13Xs	—
131	GPIO[29]	I/O	Hu	13Xs	—
132	GPIO[30]	I/O	Hu	13Xs	—

Table 1. SCE 176-Pin TQFP Assignments (Cont'd)

Pin	Signal Label	I/O	Input Type	Output Type	Pin Description
133	GPIO[31]	I/O	Hu	13Xs	—
134	GPIO[32]	I/O	Hu	13Xs	—
135	GPIO[33]	I/O	Hu	13Xs	—
136	GPIO[34]	I/O	Hu	13Xs	—
137	GPIO[35]	I/O	Hu	13Xs	—
138	GPIO[36]	I/O	Hu	13Xs	—
139	VDD	—	—	—	VDDi
140	GPIO[0]/SR4IN	I/O	Hu	13Xs	—
141	GPO[31]/SR3OUT	O	—	13Xs	—
142	GPIO[37]/IRQ15n	I	Hu	13Xs	—
143	IARESET	O	—	13Xs	DSP to EXTIA POR
144	IACLK/DSPCSn	O	—	13Xs	DSP to EXTIA MCLK/Ext. Modem CSn
145	IA1CLK	I	H	—	DSP from EXTIA ICLK
146	SR3IN/DSPIRQn	I	H	—	DSP from primary EXTIA SOUT/EXT. Modem IRQn (Used only for optional Line IA in place of SmartDAA.)
147	SR4OUT	O	—	13Xs	DSP to primary EXTIA SIN (Used only for optional Line IA in place of SmartDAA.)
148	SR1IO	O	—	13Xs	DSP to EXTIA CTRL1
149	SA1CLK	I	H	—	DSP from EXTIA FSYNC
150	VSS	—	—	—	VSSi for PLL
151	TSTCLK	O	—	13Xs	—
152	DEBUGn	I	Hu	—	—
153	RDn	O	—	13Xs	—
154	WRn	O	—	13Xs	—
155	SYNC/GPO[20]	O	—	13Xs	—
156	ROMCSn	O	—	13Xs	—
157	CS1n/GPO[21]	O	—	13Xs	—
158	VSS	—	—	—	VSSo
159	SXIN	O	OSCO	—	—
160	SXOUT	O	—	OSCO	—
161	VDD	—	—	—	VDDo
162	PM[3]/GPO[3]	O	—	13Xs	—
163	PM[2]/GPO[2]	O	—	13Xs	—
164	PM[1]/GPO[1]	O	—	13Xs	—
165	PM[0]/GPO[0]	O	—	13Xs	—
166	SM[3]/GPO[7]	O	—	13Xs	—
167	SM[2]/GPO[6]	O	—	13Xs	—
168	SM[1]/GPO[5]	O	—	13Xs	—
169	SM[0]/GPO[4]	O	—	13Xs	—
170	REGDMA/GPO[18]	O	—	13Xs	—
171	WAITn/GPO[19]	O	—	13Xs	—
172	VDD	—	—	—	VDDi for PLL
173	D[7]	I/O	Tu	13Xs	—
174	D[6]	I/O	Tu	13Xs	—
175	D[5]	I/O	Tu	13Xs	—
176	D[4]	I/O	Tu	13Xs	—

Table 1. SCE 176-Pin TQFP Assignments (Cont'd)

<p>Notes: I/O Type Combinations</p> <ul style="list-style-type: none"> u = Pull up d = Pull down s = Slew rate control h = hysteresis t = non-hysteresis input 13X = Programmable drive 1X or 3X 1XC = 3 V CMOS output 1X drive 2XC = 3 V CMOS output 2X drive 3XC = 3 V CMOS output 3X drive 4XC = 3 V CMOS output 4X drive Osc0 = System Oscillator pad Osc1 = RTC Oscillator pad 	<p>Where:</p> <p>13X s</p> <p> Slew Rate Control</p> <p> 1X or 3X drive</p>
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Table 2. SCE Current and Power Requirements

Device	Voltage ¹	Typical Current @25°C ³	Maximum Current @ 0°C ³	Typical Power @25°C ³	Maximum Power @ 0°C ³
SCC					
Primary Power	+3.3 V ± 0.3 V	tbd mA	tbd mA	tbd mW	tbd mW
Battery Power and RTC ²	+2.7 to VDD	tbd µA	tbd µA	tbd µW	tbd µW
<p>Notes:</p> <ol style="list-style-type: none"> Input voltage ripples =0.1 volts peak-to-peak. The amplitude of any frequency between 20 KHz and 150 KHz must be less than 500 microvolts peak. Real-Time Clock (RTC) battery power measurements made with a 32.768 KHz crystal oscillator. Normal mode 					

Table 3. SCE Absolute Maximum Ratings

Parameter	Symbol	Limits	Units
Supply Voltage	V _{DD}	-0.5 to + 4.6	V
Input Voltage	V _{IN}	-0.5 to + 4.6	V
Operating Temperature Range	T _A	-0 to +70	°C
Storage Temperature Range	T _{STG}	-55 to +125	°C
Analog Inputs	V _{IN}	-0.3 to (+3.3 V +0.3 V)	V
Voltage Applied to Outputs in High Impedance (Off) State	V _{HZ}	-0.5 to + 4.6	V
DC Input Clamp Current	I _{IK}	±20	mA
DC Output Clamp Current	I _{OK}	±20	mA
Static Discharge Voltage (25°C)	V _{ESD}	±2500	V
Latch-up Current (25°C)	I _{TRIG}	±200	mA

Table 4. Crystal Specifications - 32.256 MHz Functional Mode

Characteristic	HC49U-32.256-FL	HC49U-32.256-L
Conexant Part No.		
Electrical		
Frequency	32.256 MHz nominal	32.256 MHz nominal
Frequency Tolerance	±50 ppm ($C_L = 18$ pF)	±50 ppm ($C_L = 18$ pF)
Frequency Stability		
vs. Temperature	±35 ppm (-20°C to 70°C)	±35 ppm (-20°C to 70°C)
vs. Aging	±15 ppm/5 years	±15 ppm/5 years
Oscillation Mode	Fundamental	Third Overtone
Calibration Mode	Parallel resonant	Parallel resonant
Load Capacitance, C_L	18 pF nom.	18 pF nom.
Shunt Capacitance, C_O	7 pF max.	7 pF max.
Series Resistance, R_1	35 Ω max. @100 nW drive level	40 Ω max. @100 nW drive level
Drive Level	100 μ W correlation; 500 μ W max.	100 μ W correlation; 1.0 mW max.
Operating Temperature	0°C to 70°C	-20°C to 70°C
Storage Temperature	-40°C to 85°C	-40°C to 85°C
Mechanical		
Holder Type	SMT	Through Hole
Third Lead	Required	Required
Notes:		
1. Characteristics @ 25°C unless otherwise noted.		
2. Suggested supplier:		
ILSI America		
5458 Louie Lane		
Reno, NV 89511		
USA		
(702) 851-8880		

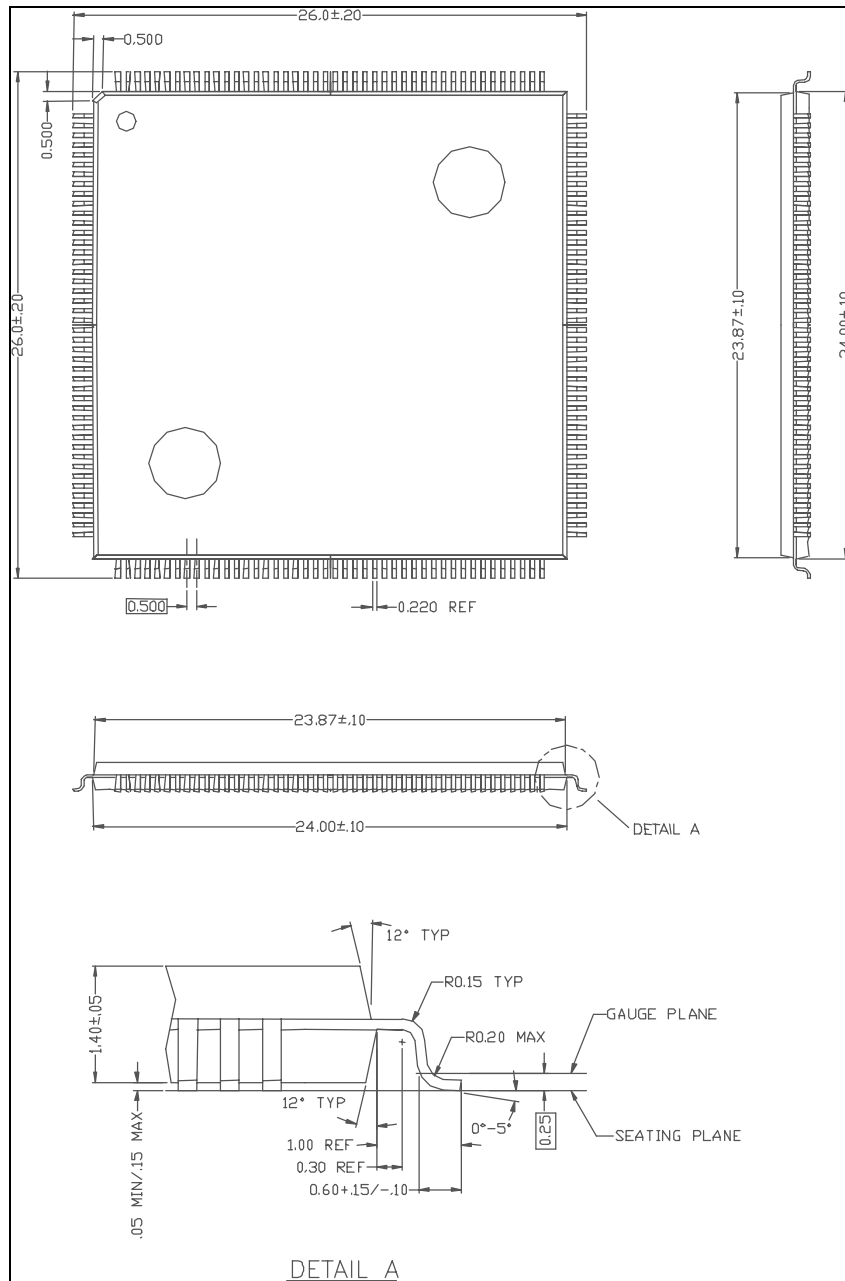


Figure 3. 176-Pin TQFP Package Dimensions



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